

Conventional poly-Si gate MOS-transistors with a novel, ultra-thin Hf-oxide layer

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Abstract

Conventional poly-Si gate MOS transistors with a high-k gate-dielectric were fabricated using a novel, ultra-thin Hf-oxide. Various integration effects on the high-k layer were studied such as Si-surface preparation, deposition conditions, and post-deposition anneals, demonstrating EOT of 1.6 to 1.2 nm and excellent gate leakage current. Promising transistor behaviors were obtained including electron mobility up to 90% of SiO₂ at both peak and high-field.