Robust Memory Cell Capacitor using Multi-Stack Storage Node for High Performance in 90nm Technology and Beyond

*****Jaegoo Lee, Yongseok Ahn, Yangkeun Park, Minsang Kim, Dongjun Lee, Kyuhyun Lee, Changhyun Cho, Taeyoung Chung and Kinam Kim

Advanced Technology Development Team, Memory Division, Device Solution Network, Samsung Electronics Co.,
San #24, Nongseo-Lee, Kiheung-Eup, Yongin-City, Kyungki-Do, Korea
Tel) 82-31-209-5390, Fax)82-31-209-3274, E-mail)amusante@samsung.co.kr**.**

Abstract

90 nm DRAM technology and beyond requires the robust memory cell capacitor structure in order to increase cell capacitance for high performance and low power applications. Thus, the cell technology must have the feature of high capacitance of memory cell capacitor while maintaining its mechanical stability. To accomplish these purposes, we develop the multi-stack storage node structure whose enlarged bottom size of OCS(**O**ne **C**ylindrical **S**torage node) can give much better mechanical stability of the capacitor than that of the conventional capacitor. Using Al_2O_3/HfO_2 dielectric material together with this structure can give high cell capacitance 30fF/cell and low leakage current less than 1fA/cell.