A Functional 0.69µm² Embedded 6T-SRAM bit cell for 65nm CMOS platform

This work highlights a 65nm CMOS integration for low power and general-purpose applications. A 6-T SRAM cell size of 0.69um² with a 45nm gate length is demonstrated. Functional SRAM bit-cell is presented using a conventional nitrided gate oxide dielectric. A comparison between offset spacer and PLAsma Doping (PLAD) is made for the transistor characteristics with very promising V_{th}-L_d and profiles measured. Lithography employed a combination of both optical lithography and e-beam imaging. The BEOL integration used a conventional low K dielectric with copper metallization.