

75 Word Abstract

Ultra Low Power 6T-SRAM Chip with Improved Transistor Performance and Reliability by HfO₂-Al₂O₃ High-k Gate Dielectric Process Optimization

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Ultra low power 6T-SRAM chips with HfO₂-Al₂O₃ laminate gate dielectric were successfully demonstrated (bit-cell size = 2.14 μm², EOT = 1.56 nm). Carrier mobility, reliability characteristics of TDDDB and HCI, and flicker noise of the thin high-k transistors were improved by deliberate optimizing the conditions of post nitridation, and PDA (O₂ + N₂) temperature. For the thin high-k 6T-SRAM, SNM, cell delay, and chip yield were comparable to those of the oxynitride device while dynamic power was more than 2 orders low.