A 65nm-node CMOS Technology with Highly Reliable Triple Gate Oxide Suitable for power-considered System-on-a-Chip

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We have developed 65nm-node CMOS technology for general-purpose system-on-a-chip, in which both standby and active power reductions are strongly required. With highly reliable triple gate oxide and optimized RTA condition, an average standby current can be reduced to one-fifth compared with conventional case. High-speed and low-gate-leakage transistors show on-current (n/p) of 680/240μA/μm with I_G 13nA/μm and I_{OFF} 30nA/μm and of 490/175μA/μm with I_G 0.8nA/μm and I_{OFF} 3nA/μm, simultaneously. Gate oxide of all the above transistors exhibit tight TDDB distributions.