(110)-Surface Strained-SOI CMOS Devices with Higher Carrier Mobility

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We have developed (110) strained-SOI *n*- and *p*-MOSFETs on (110) relaxed-SGOI with the Ge content of 25% for higher performance, applying the Ge condensation technique to SiGe layers on (110) SOI wafers. We have demonstrated, for the first time, that the electron and the hole mobility enhancements of (110) strained-SOI devices amount to 23% and 50%, respectively, against to the carrier mobilities of (110) unstrained MOSFETs. The carrier mobilities of (110) strained-SOI strongly depend on the current flow directions. As a result, the electron and the hole mobility ratios of (110) strained-SOI MOSFETs to the universal mobility of (100) bulk-MOSFETs increase up to 81% and 203%, respectively. Especially, this (110) hole mobility enhancement is larger by about 50% than that of (100) strained-SOI, and the current drive unbalance between *n*- and *p*-MOS can be reduced. Therefore, (110)-surface strained-SOI technology is also the candidate for higher speed scaled CMOS, optimizing the current flow directions of *n*- and *p*-MOS.