Performance of 70nm Strained-Silicon CMOS Devices

J.R. Hwang, J.H. Ho, S. M. Ting, T.P. Chen, Y.S. Hsieh, C.C. Huang, Y.Y. Chiang, H.K. Lee, Ariel Liu, T.M. Shen, G. Braithwaite[+], M.T. Currie[+], N. Gerrish[+], R. Hammond[+], A. Lochtefeld[+], F. Singaporewala[+], M.T. Bulsara[+], Q. Xiang*, M.R. Lin*, W.T. Shiau, Y.T. Loh, J.K. Chen, S.C. Chien, S.W. Sun and Frank Wen

[+]AmberWave Systems, 13 Garabedian Drive, Salem, NH 03079, USA
*Strategic Technology, AMD, One AMD Place, Sunnyvale, CA 94088, USA
Central Research and Development Division, UMC,
No. 3, Li-Hsin Rd. II, Hsin-Chu City, Taiwan 30077 (w_t_shiau@umc.com)

An 86% electron mobility improvement and 20% $I_{dn\text{-}sat}$ enhancement were demonstrated for a 70nm strained-Si CMOS process fabricated on SiGe virtual substrates. Compared to bulk CMOS, strained-Si CMOS delivered 95% higher inverter peak-current and 2.2ps reduced ring oscillator delay for the same drive current. Strained and bulk CMOS featured equivalent gate leakage although higher dislocation-induced junction leakage on strained-Si was observed. Self-heating due to the lower thermal conductivity of SiGe reduces $I_{dn\text{-}sat}$ by 7% during DC operation.