SESSION 11 – TAPA II
Non-Volatile FinFet Flash Memory

Wednesday, June 14, 10:25 a.m.
Chairpersons: T.-J. King Liu, Synopsys, Inc.
J. T. Moon, Samsung Electronics Co., Ltd.

11.1 – 10:25 a.m.
Paired FinFET Charge Trap Flash Memory for Vertical High Density Storage, S. Kim, W. Kim, J. Hyun, S. Byun, J. Koo, J. Lee, K. Cho, S. Lim, J. Park, I.-K. Yoo, C.-H. Lee*, D. Park*, Y. Park, Samsung Advanced Institute of Technology, Gyeonggi-Do, Korea, *Samsung Elec. Co., Gyeonggi-Do, Korea

A new type of memory, Paired FinFET charge trap memory is reported. It consists of two split silicon fins and insulator between them. Two channels are formed on the outer surface of silicon so doubled integration density can be achieved. We successfully fabricated Paired FinFET SONOS devices. It shows good program and erase characteristics. Independent programming on each storage nodes is demonstrated. The circuit configuration for NAND flash application is also proposed.

11.2 – 10:50 a.m.
SONOS-type FinFET Device Using P^+ Poly-Si Gate and High-k Blocking Dielectric Integrated on Cell Array and GSL/SSL for Multi-Gigabit NAND Flash Memory, S.-K. Sung, S.-H. Lee, B.Y. Choi, J.J. Lee, J.-D. Choe, E.S. Cho, Y.J. Ahn, D. Choi, C.-H. Lee, D.H. Kim, Y.-S. Lee, S.B. Kim, D. Park, B.-I. Ryu, Samsung Electronics Co., Gyeonggi-Do, Korea

For the multi-gigabit NAND Flash memory, SONOS-type FinFET device with p^+ gate and high-k blocking dielectric has been integrated both on the cell array and GSL/SSL for the first time. The advantages of the FinFET structure for the NAND Flash application have been theoretically and experimentally demonstrated, and the results show that the 85 % improved on-cell current is achievable using FinFET device. The enhanced programming and retention characteristics of FinFET have been also presented, and modeled by the potential changes on fully-depleted body of the sub-40 nm ultra-narrow fin.

11.3 – 11:15 a.m.
Trap Layer Engineered FinFET NAND Flash with Enhanced Memory Window, Y.J. Ahn, J.-D. Choe, J.J. Lee, D. Choi, E.S. Cho, B.Y. Choi, S.-H. Lee, S.-K. Sung, C.-H. Lee, S.H. Cheong, D.K. Lee, S.B. Kim, D. Park, B.-I. Ryu, Samsung Electronics Co., Gyeonggi-Do, Korea

This paper presents the trap layer engineered body-tied FinFET device for MLC NAND Flash application. The device design parameters for high density NAND Flash memory have been considered, and the advantages of FinFET structure and high-k blocking dielectric in such device have been demonstrated. Based on the WN nano-dot memory device, the trap layer engineering using nitride layer has been performed, and the results show that the memory window is improved from 2.6 V to 7.8 V by utilizing engineered trap layer at 14 MV/cm F-N programming, and it is proposed as a possible MLC NAND device structure.

11.4 – 11:40 a.m.
Technology Breakthrough of Body-Tied FinFET for Sub 50 nm NOR Flash Memory, E.S. Cho T.-Y. Kim, B.K. Cho, C.-H. Lee, J.J. Lee, A. Fayrushin, C. Lee, D. Park, B.-I. Ryu, Samsung Electronics Co., Gyeonggi-Do, Korea

We have achieved an optimal scheme for the practical application of Body-Tied FinFET for sub 50 nm NOR Flash memory. Using this scheme, high program speed (Vt>8V@1μs) and low drain disturbance (DVt=-0.1V@5ms) with a good reliability have been demonstrated. The effects of USC (ultra-shallow conformal) doping and SGHE (secondary generated hot electron) injection on program and drain disturbance characteristics of FinFET cells have been intensively studied. In addition, the (100) channel engineered Body-Tied FinFET shows manufacturable endurance characteristics.