SESSION 13 – TAPA II
Analog/RF/Mixed-Signal VLSI

Wednesday, June 14, 1:30 p.m.
Chairpersons: C. Bulucea, National Semiconductor Corp.
T. Dan, Sanyo Electric Co., Ltd.

13.1 – 1:30 p.m.
A 45nm Low Cost Low Power Platform by Using Integrated Dual-Stress-Liner Technology, J. Yuan, S.S. Tan[1], Y.M. Lee[1], J. Kim[2], R. Lindsay[3], V. Sardesai, T. Hook, R. Amos, Z. Luo, W. Lee[1], S. Fang, T. Dyer, N. Rovedo, R. Stierstorfer[3], Z. Yang, J. Li, K. Barton, H. Ng, J. Sudijono[1], J. Ku[2], M. Heirlemann[3], T. Schiml[3], IBM Semiconductor Research and Development Center, Hopewell Junction, NY, [1]Chartered Semiconductor Manufacturing Limited, [2]Samsung Electronics Co. Ltd., [3]Infineon Technologies AG

Device performance has been boosted by integrating dual-stress-liners (DSL) in a 45nm low power platform as a cost effective approach. A stress-proximity-technique (SPT) has been explored to improve device performance without adding process complexity. Record drain currents of 840/490 uA/um have been achieved for NMOS and PMOS, respectively, at 1.2V and off-leakage current of 1nA/um. Junction profiles have been optimized to reduce the gate-induced-drain-leakage (GIDL). An asymmetric IO has been integrated into this low power technology for the first time, offering multiple advantages including low cost, performance gain up to 30% and reliability improvement as well.

13.2 – 1:55 p.m.
High Performance Micro-Crystallized TaN/$SrTiO_3$/TaN Capacitors for Analog and RF Applications, K.C. Chiang, C.C. Huang, A. Chin, W.J. Chen*, H.L. Kao, M. Hong**, J. Kwo**, National Chiao-Tung University, Hsinchu, Taiwan, *National Ping-Tung University of Science and Technology, Taiwan, **National Tsing Hau University, Hsinchu, Taiwan

Using micro-crystallized high-k $SrTiO_3$ on N± treated TaN, very high 28 fF/um^2 capacitance density, low voltage linearity of 92 ppm/V2 and small leakage of 3x10-8 A/cm^2 at 2V are beyond ITRS spec of Analog capacitor at year 2018. Further improving to 44 fF/um^2 and low VCC of 54 ppm/V^2 are obtained for higher speed Analog/RF ICs at 2 GHz.

13.3 – 2:20 p.m.
Improved 1/f Noise Characteristics in Locally Strained Si CMOS using Hydrogen-Controlled Stress Liners and Embedded SiGe, T. Ueno, H.S. Rhee, H. Lee, M.S. Kim, H.S. Cho*, H.S. Baik*, Y.H. Jung, H.W. Lee, H.S. Park, C.K. Lee, G.-J. Bae, N.-I. Lee, Samsung Electronics Co. Ltd., Kyunggi-Do, Korea, *SAIT, Kyunggi-Do, Korea

1/f noise improvement for a locally strained Si MOS with hydrogen-controlled stress liners and eSiGe has been demonstrated for the first time. The noise is reduced because the applied strains decrease the carrier mass without generating additional interface states. A high hydrogen density of $1x10^2$ $2cm^{-3}$ in a stress liner increases the noise, while eSiGe drastically reduces the noise by stressing the channel without hydrogen incorporation.

13.4 – 2:45 p.m.
Impact of HfSiON Induced Flicker Noise on Scaling of Future Mixed-Signal CMOS, Y. Yasuda[1,2], C.-H. Lin[1], T.-J. King Liu[1], C. Hu[1], [1]University of California, Berkeley, California, [2]NEC Electronics Corporation

It is shown for the first time that HfSiON gate dielectric thickness has a strong impact on the flicker (1/f) noise of devices with Lg < 1μm. We have developed a simple model for both gate length (Lg) and HfSiON thickness dependences of N-FET flicker noise, based on excess traps at the gate-edges. P-FET noise does not exhibit such strong dependences. Scaling of future analog devices with high-k gate stack may be limited by noise considerations.