SESSION 21 – HONOLULU SUITE
Front-End of Line Processing

Thursday, June 15, 1:30 p.m.
Chairpersons: K. Schruefer, Infineon
Y. Takao, Fujitsu Ltd.

21.1 – 1:30 p.m.
Enhanced Performance of PMOS MUGFET via Integration of Conformal Plasma-Doped Source/Drain Extensions, D. Lenoble, K. G. Anil, A. De Keersgieter, P. Eybens, N. Collaert, R. Rooyackers, S. Brus, P. Zimmerman, M. Goodwin, D. Vanhaeren, W. Vandervorst, S. Radovanov[1], L. Godet[1,2], C. Cardinaud[2], S. Biesemans, T. Skotnicki[3], M. Jurczak, IMEC, Leuven, Belgium, [1]VSEA, Gloucester, MA, [2]Nantes University, France, [3]STMicroelectronics, Alliance, France

For the first time, scaled PMOS MUGFET devices with TiCN/HfO_2 gate stack is doped with specific pulsed plasma doping processes. This paper first highlights the key benefit brought by conformal source/drain extensions, demonstrates how pulsed plasma doping process can be tuned to conformally dope very dense Fin structures and finally shows that high performance (+24% vs. ion implant reference) multi-gate pMOS device (720 µA/µm @ Ioff=20nA/µm, at Vds=-1.2V) is achieved with extensions formed by optimized PLAD process.

21.2 – 1:55 p.m.
RTA-Driven Intra-Die Variations in Stage Delay, and Parametric Sensitivities for 65nm Technology, I. Ahsan, N. Zamdmer, O. Glushchenkov, R. Logan, E.J. Nowak[1], H. Kimura[2], J. Zimmerman[1], G. Berg, J. Herman, E. Maciejewski, A. Chan, A. Azuma[3], S. Deshpande, B. Dirahoui, G. Freeman, A. Gabor, M. Gribelyuk, S. Huang, M. Kumar, K. Miyamoto[3], D. Mocuta, A. Mahorowala, E. Leobandung, H. Utomo, B. Walsh, IBM Systems and Technology Group, Hopewell Junction, NY, [1]IBM Semiconductor Research and Development Center, Essex Junction, VT, [2]Sony Electronics Inc., Hopewell Junction, NY, [3]Toshiba America Electronic Component Inc., Hopewell Junction, NY

We report, for the first time, a detailed study of Intra-Die Variation (IDV) of CMOS inverter delay for the 65nm technology, driven by mm-scale variations of rapid thermal annealing (RTA). We find that variation in VT and REXT accounts for most of the IDV in delay and leakage and is modulated by RTA ramp rate. We show a good correlation of inverter delay to mm-scale variation in the predicted reflectivity of the device pattern densities.

Keywords: CMOS, RTA, Variation, and Ramp Rate

21.3 – 2:20 p.m.
Performance Enhancement in 45-nm Ni Fully-Silicided Gate/High-k CMIS using Substrate Ion Implantation, Y. Nishida, T. Yamashita, S. Yamanari, M. Higashi, K. Shiga, N. Murata, M. Mizutani, M. Inoue, S. Sakashita, K. Mori, J. Yugami, T. Hayashi, A. Shimizu, H. Oda, T. Eimori, O. Tsuchiya, Renesas Technology Corp., Hyogo, Japan

High performance Ni-FUSI/HfSiON CMIS with suitable Vth in a wide Lg range is presented. This is accomplished by ion implantation to substrate and phase control of Ni-FUSI gate. Threshold voltage of NiSi-FUSI NMIS is controlled by nitrogen implantation, and that of Ni_2Si-FUSI PMIS is controlled by fluorine implantation. It is demonstrated that N/F incorporation can realize 0.2-V-low |Vth|, high carrier mobility, and high reliability for both NMIS and PMIS. Drain current increases by 16% for NMIS and by 55% for PMIS compared with poly-Si/high-k CMIS. Substrate ion implantation engineering is promising for multi-Vth CMIS platform for 45-nm node and beyond.

21.4 – 2:45 p.m.
Channel Stress Modulation and Pattern Loading Effect Minimization of Milli-Second Super Anneal for Sub-65nm High Performance SiGe CMOS, C.-H. Chen, C.F. Nieh, D.W. Lin, K.C. Ku, J.C. Sheu, M.H. Yu, L.T. Wang, H.H. Lin, H. Chang, T.L. Lee, K. Goto, C.H. Diaz, S.C. Chen, M.S. Liang, Taiwan Semiconductor Manufacturing Co. Ltd.

In this paper, we present an advanced integration approach using milli-second anneal technique to enhance device performance. In addition to enhanced poly-silicon activation, the device gain resulted from channel stress modulation, and retarded dopant diffusion can be obtained through process optimization including rapid-thermal anneal (RTA), capping layer, and milli-second anneal. More than 15% NMOS performance gain is demonstrated without undergoing milli-second-anneal-induced pattern loading effect and re-crystallization defect. No obvious stress relaxation and driving current degradation are observed in epi-SiGe PMOS. Moreover, the performance gain is increased while lowering the RTA temperature, suggesting that our proposed approach may open an alternative pathway for 45nm technology node and beyond.