SESSION 22 – TAPA I
Novel Gate Stacks Engineering
and Characterization

Thursday, June 15, 3:25 p.m.
Chairpersons: D. Gravesteijn, Philips Research Leuven
C. C. Wu, TSMC

22.1 – 3:25 p.m.
Novel Stack-SIN Gate Dielectrics for High Performance 30 nm CMOS for 45 nm Node with Uniaxial Strained Silicon, H. Ohta, M. Hori, M. Shima*, H. Mori, Y. Shimamune*, T. Sakuma, A. Hatada*, A. Katakami*, Y. Kim, K. Kawamura, T. Owada, H. Morioka, T. Watanabe, Y. Hayami, J. Ogura, N. Tamura*, M. Kojima, K. Hashimoto, Fujitsu Limited, Tokyo, Japan, *Fujitsu Laboratories Ltd., Tokyo, Japan

Aggressively scaled 30nm gate CMOSFETs for 45nm node is reported. We successfully improved a higher drive current with keeping the short channel effect by S shaped SiGe-Source/Drain (S SiGe) structure using compressive-stressed liner. In addition, we developed Novel stack-SIN gate dielectrics by using Bis-TertiaryButylAmino-Silane (BTBAS)/NH3. Novel stack-SIN gate dielectrics show higher immunity to negative bias temperature instability (NBTI) and Time-Dependent Dielectric Breakdown (TDDB) lifetime compared with conventional plasma nitrided silicon dioxide. These characteristic are originated from its unique nitrogen profile. The nitrogen concentration is over 22% at the surface of the dielectric and it rapidly decreases to 1% at the interface with a substrate. A high performance 30 nm gate nMOSFET and pMOSFET were demonstrated with a drive currents of 1042 mA/mm and 602 mA/mm at Vd=1 V / Ioff=100 nA/mm, respectively.

22.2 – 3:50 p.m.
Band-Edge High-Performance High-*k*/Metal Gate n-MOSFETs using Cap Layers Containing Group IIA and IIIB Elements with Gate-First Processing for 45 nm and Beyond, V. Narayanan, V.K. Paruchuri, N.A. Bojarczuk, B.P. Linder, B. Doris, Y.H. Kim, S. Zafar, J. Stathis, S. Brown, J. Arnold, M. Copel, M. Steen, E. Cartier, A. Callegari, P. Jamison, D.L. Lacey, Y. Wang*, P.E. Batson, P. Ronsheim*, R. Jammy, M.P. Chudzik, M. Ieong, S. Guha, G. Shahidi, T.C. Chen, IBM Semiconductor Research and Development Center, Yorktown Heights, NY, *IBM Systems and Technology Division, Hopewell Junction, NY

We have fabricated electrically reliable band-edge (BE) high-k/Metal nMOSFETs stable to 1000ºC, that exhibit the highest mobility (203 cm^2/Vs @ 1MV/cm) at the thinnest Tinv (1.4 nm) reported to date. These stacks are formed by capping HfO_2 with ultra-thin layers containing strongly electropositive gp. IIA and IIIB elements (e.g. Mg and La) prior to deposition of the TiN/Poly-Si electrode stack, in a conventional gate-first flow. Short channel devices with band edge characteristics are demonstrated down to 60 nm.

22.3 – 4:15 p.m.
Two Different Mechanisms for Determining Effective Work Function ($\Phi_{m,eff}$) on High-k - Physical Understanding and Wider Tunability of $\Phi_{m,eff}$ -, M. Kadoshima, A. Ogawa, H. Ota*, M. Ikeda, M. Takahashi, H. Satake, T. Nabatame, A. Toriumi*,#, MIRAI-ASET, Ibaraki, Japan, *MIRAI-ASRC, Tsukuba, Japan, #The University of Tokyo, Tokyo, Japan

We have experimentally found two different mechanisms characterizing effective work function ($\Theta_{m,eff}$) of a gate electrode on Hf-based high-k dielectrics. Interface dipoles induce both positive and negative $\Theta_{m,eff}$ shifts. The positive shift is almost independent of gate electrode materials, while the negative one is sensitive to Si composition of the gate electrode. By making the most of two types of interface dipoles, $\Theta_{m,eff}$ of gate electrodes on Hf-based high-k can be widely tuned for further advanced scaled CMOS.

22.4 – 4:40 p.m.
Sub-1Å-Resolution Analysis and Physical Understanding of Gate/Insulator Interfacial Region in Scaled-T_{inv} High-k Gate Stacks, M. Saitoh, Y. Tsuchiya, Y. Kamimuta, T. Saito, K. Sekine, T. Kobayashi, T. Aoyama, M. Koyama, A. Nishiyama, Toshiba Corporation, Yokohama, Japan

We propose sub-1Å-order analysis of gate/insulator interfacial region in scaled-T_{inv} gate stacks by differentiatng their C-V curves. By applying this technique to p+poly-Si/HfSiON, it is found that gate depletion increases due to both lower poly impurity conc. (Npoly) and huge amount of pinning charge inside the dielectric (Nox). We found ultra-thin SiN cap insertion recovers the degradation in Npoly and Nox, leading to improvement of gate depletion and DVfb. By analyzing FUSI stacks, absence of semiconducting interlayer is verified with sub-1Å-resolution, and it is also found that As segregation outside SiO_2 leads to EOT increase as well as workfunction (WF) modulation in As-doped FUSI/SiO_2, whereas As segregation inside HfSiON results in smaller WF change in FUSI/HfSiON.