SESSION 23 – HONOLULU SUITE
Advanced Source/Drain Engineering

Thursday, June 15, 3:25 p.m.
Chairpersons: M. Mirabedini, LSI Logic Corp.
H. Wakabayashi, NEC Corp.

23.1 – 3:25 p.m.
Novel Approach to Reduce Source/Drain Series Resistance in High Performance CMOS Devices Using Self-Aligned CoWP Process for 45nm Node UTSOI Transistors with 20nm Gate Length, J. Pan, A. Topol*, I. Shao*, D. Singh* Z. Ren*, C.-Y. Sung*, M. Ieong*, J. Pellerin, J. Iacoponi, M.-R. Lin, AMD Corporation, Hopewell Junction, NY, *IBM T. J. Watson Research Center, Yorktown Heights, NY

This paper reports a novel, non-epitaxial raised source/drain approach to decrease the series resistance in nMOSFETs fabricated on UTSOI using a selective electroless metal deposition process. A metallic layer selectively deposited in the source/drain nickel or cobalt silicide regions significantly reduces the series resistance in nMOSFETs with 10nm body thickness and gate lengths down to 20nm. The extremely high selectivity of the process is confirmed through gate leakage measurements.

23.2 – 3:50 p.m.
Advanced Junction Profile Engineering Featuring Laser Spike Annealing and Co-implantation for Sub-30-nm Strained CMOS Devices, T. Yamamoto, T. Kubo, T. Sukegawa, K. Hashimoto, M. Kase, Fujitsu Ltd., Tokyo, Japan

We have developed a novel junction profile engineering using laser spike annealing (LSA) with co-implant and applied it to sub-30-nm strained CMOS devices. A 55% reduction in source-drain extension (SDE) resistance achieves a 15% improvement in the saturation on-current (Ion) at a 28-nm gate length for PMOS. A reduction in the source-drain parasitic resistance enables an over 50% improvement in the linear on-current (Idlin) by capping layer stress on the 29-nm gate length, which is about a 10% increase in the Idlin improvement ratio compared to that of the control device, and a 28% of Ion enhancement gave us Ion= 460 uA/um for Ioff= 100 nA/um at Vd= -1.0 V. For NMOS, low resistance SDE can be obtained without inducing the deterioration of the Vth-rolloff thanks to the halo profile modulation, and 6% of Ion enhancement was achieved at a 29-nm gate length, and I_{on}= 925 uA/um for I_{off}= 100 nA/um at Vd= 1.0 V was obtained.

23.3 – 4:15 p.m.
Unique Ultra Shallow Junction Scheme with Conventional Activation Process, C.H. Tsai, B.C. Lan, Y.H. Lin, W.T. Chiang, T.Y. Chang, P.W. Liu, J.W. Pan, Y.C. Liu, J.L. Tsai, T.F. Chen, C.T. Tsai, United Microelectronics Corporation, Hsin-Chu City, Taiwan

A unique ultra shallow junction scheme featured with integrating diffusion barrier into eSiGe:B strained pMOSFETs has been demonstrated. Embedded diffusion barrier (EDB) drastically suppresses boron out-diffusion from subsequent thermal treatment, thus resulting in superior short channel control. This approach enables the formation of ultra shallow junction, over 30% junction depth reduction, while simultaneously maintaining low extension resistance using conventional activation process only. Furthermore, eSiGe:B with embedded diffusion barrier (eSiGe:B w/ EDB) scheme can still retain local stress and enhanced pMOSFETs current. Device performance and barrier layer characteristics of eSiGe:B w/ EDB scheme are also reported in this work.

23.4 – 4:40 p.m.
A Raised Source/Drain Extension pFET on Si (110) Realized by In-situ Doped Selective Epitaxy Technology, J. Wang, Y. Kikuchi, Y. Tateshita, T. Kato, T. Kataoka, T. Hirano, K. Nagano, T. Ikuta, Y. Miyanami, S. Fujita, S. Hiyama, R. Yamamoto, S. Kanda, S. Yamakawa, T. Kimura, K. Kugimiya, N. Yamagishi, Y. Tagawa, Y. Kamide, H. Iwamoto, T. Ohno, M. Saito, S. Kadomura, N. Nagashima, Sony Corporation, Kanagawa, Japan

A raised source/drain extension (RSDE) pFET on (110) Si wafer is demonstrated for the first time with in-situ doped selective epitaxy technology. Roll-off has been effectively improved, resulting from the elimination of ion channeling in (110) Si. Due to the hole mobility enhancement and parasitic resistance reduction, Ion of 389 uA/um (Vd = -1.0 V) is achieved at Lmin of around 30nm extracted from the Ioff = 100 nA/um, which is 83% higher than that of conventional planar (100) pFET.