2006 VLSI Technology Short Course
TAPA I/II

Process Technologies for Continued Scaling and Performance

Monday, June 12, 2006, 9:00 a.m.

Organizers: Robert Chau, Intel Corporation
Toshihiro Sugii, Fujitsu Laboratories, Ltd.

9:00 a.m. **Back-end Interconnect Technology**
C.H. Jan, Intel Corp.

10:00 a.m. **Break**

10:15 a.m. **Advanced Embedded Memories**
K. Ishimaru, Toshiba Corp.

11:15 a.m. **Lithography Solutions for 32nm and Beyond**
M. Kameyama, Nikon Corp.

12:15 p.m. **Lunch**

2:00 p.m. **Ultra-Shallow Junction Technologies**
M. Kase, Fujitsu, Ltd.

3:00 p.m. **Device Technology**
S. Thompson, University of Florida

4:00 p.m. **Break**

4:15 p.m. **High-k Gate Dielectrics**
J. Lee, University of Texas at Austin

5:15 p.m. **Conclusion**