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For Immediate Release

Breakthroughs in Transistors, Interconnects & Integrated Circuit Technology for Computing, Memory and Communications, including Medical, Power, Automotive and More, to be Highlighted at the 2013 Symposia on VLSI Technology and Circuits

- *Premier mid-year gatherings for microelectronics engineers, managers and researchers*
- *Joint technology and circuits focus sessions introduced in2012will be continued*
- *More than 200 presentations at the leading edge of electronics technology*
- *Executive Panel Session will be held as a memorial for Prof. Shoji Tanaka, one of the founders of the Symposia on VLSI Technology and Circuits*

KYOTO, JAPAN (April 10, 2013) -- About 1,000 of the world's leading experts in the field of microelectronics will gather here for the 2013 Symposia on VLSI Technology and Circuits, from June 11-13, 2013 (Technology) and from June 12-14, 2013 (Circuits). The Symposia alternate between here and Honolulu, HI annually and serve as the premier mid-year gatherings to present research for the advancement of microelectronics technology and circuit development.

To foster joint interactions among device technologists and circuit/system designers, the technical programs of both Symposia will overlap for two days, and attractive joint technology-circuits focus sessions - which were successfully introduced in last year - will be held again. For a single registration fee, attendees can benefit from unique opportunities for interdisciplinary learning that cannot be replicated by other important conferences in each area.

More than 200 presentations will be given, including short courses prior to each Symposium, invited speakers addressing the industry's most important issues, evening rump sessions spanning a range of topics at the leading edge of technology and circuit design, and a compelling luncheon talk. Also, the Symposium on VLSI Technology will be preceded by the Silicon Nanoelectronics Workshop on June 09-10, 2013 and the Spintronics Workshop on LSI in the evening of June 10, 2013

"This year's VLSI Technology program will highlight the breakthroughs in the evolution of SoC and More-than-Moore technologies such as advanced CMOS devices, eDRAM, new NVM's, image sensor, and their processes (lithography, interconnects and 3D stacks), as the semiconductor industry is moving to the beyond 22-nm node," said Hitoshi Wakabayashi of Tokyo Institute of Technology, Symposium Chair of the 2013 Symposium on VLSI Technology.

"The VLSI Circuits program will present major advancements in the designs with scaled devices at and below 22 nm and also with three dimensional chip stacking with TSVs, as well as more universal topics such as energy-efficient electronics, bio-medical applications, and wireline/wireless communications interfaces," said Makoto Nagata of Kobe University, Symposium Chair of the 2013 Symposium on VLSI Circuits.

Both Symposium Chairs also expressed that: *"Joint focus sessions provide excellent opportunities of close interactions among technology and circuits communities, with alignments of selected topics in a program as well as a common session room for ease of participation."*

Executive Panel Session

A special "Executive Panel" session will be held this year as a memorial ceremony for Professor Shoji Tanaka to commemorate his great contributions. Prof. S. Tanaka was one of the founders of the Symposium on VLSI Technology and the Symposium Co-chair of the first Symposium in 1981. He passed away in 2011.

The executive panel(Sub-title of this panel is ***"Message for the future of VLSI"***) will be held in the morning of June 12, 2013, just after the Circuit opening session as a plenary event. Four distinguished panelists will talk about historical aspects of semiconductor technology, positive comments forecasting continuous technology advancements, and messages for young professionals in this field.

The Chair persons of this panel discussion will be Prof. C. Sodini (MIT) and Prof. T. Sakurai (Univ. of Tokyo). The panelists are Prof. T. Sugano (the Univ. of Tokyo & Toyo Univ.), Dr. S. Kohyama (Covalent Materials), Dr. D. Buss (Texas Instruments) and Prof. R. Brodersen (UC Berkeley). All participants of both Symposia are cordially invited to attend this panel session.

Plenary Sessions

The **Symposium on VLSI Technology** will open with two invited plenary talks. First, Dr. Jack Y.-C.Sun from TSMC will share his view through the presentation of ***"System Scaling and Collaborative Open Innovation"***. Then, Dr. Robert Gilmore from Qualcomm will give a talk, ***"System Design Considerations for Next Generation Wireless Mobile Devices"***.

The **Symposium on VLSI Circuits** will open with two invited plenary talks by renowned experts. First, Dr. Seh-Woong Jeong from Samsung Electronics will share his view through the presentation of ***"Perspective on Mobile Devicesand Their Impact on Semiconductor Technologies"***. Then, Dr. Peter L. Bocko from Corning will give a talk titled, ***"Glass for the Future: Displays and Semiconductors"***.

VLSI Symposia Technology/Circuits Joint Focus Sessions

The Technology/Circuits Joint Focus Sessions are devoted to advanced device and circuit design co-optimization, a key ingredient for future progress. They will have both invited papers and regular papers and will be held as all-afternoon-long sessions:

- ***Design Enablement*** (6/12/2013, Wednesday afternoon)
  Invited Speakers: H. Gossner (Intel), B. Sheu (TSMC)
- ***SRAM*** (6/13/2013, Thursday afternoon)
  Invited Speakers: T. Hook (IBM), K. Endo (AIST)

In addition, the **Symposium on VLSI Technology** will hold two special focus sessions Tuesday afternoon, June 11, 2013.

- ***3D System and Packaging***
  Invited Speakers: D. Ibbotson (Altera), Y. Orii (IBM Tokyo)
- ***3D and Emerging Memory***
  Invited Speakers: S. Muraoka (Panasonic), A. Nitayama (Toshiba)

The **Symposium on VLSI Circuits** will present two special focus sessions.

- ***3D Integrated Circuits & Applications*** (6/12/2013, Wednesday morning)
- ***Emerging Memories*** (6/13/2013, Thursday morning)

Rump Sessions

Both Symposia will sponsor a ***Joint Rump Session*** on Tuesday evening (June 11, 2013) as follows.

- "***SOC vs. 3D IC in the More-than-Moore Era"*** will be moderated by S. Ramaswami (Applied Materials) and S. Natarajan (TSMC). It will give the audience an opportunity to learn about the state-of-the-art SoC and 3D IC technologies through the panel discussions .

  Panelists: L. Madden (Xilinx), P. Franzon (UNC), C. Webb (Intel), K. Takeuchi (Chuo Univ.), W. Weber (Infineon), D. Yu (TSMC), S. Iyer (IBM)

The **Symposium on VLSI Technology** will hold two rump sessions in parallel on Tuesday evening, June 11, 2013 to foster open discussion of challenging R&D issues.

- "***Low Voltage - How low can we go?",*** moderated by A. Seabaugh (Univ. of Notre Dame) and K. Uchida (Keio Univ.), will deal with following questions: How low can we expect voltage to go for general purpose computing? What are the prospects for technologies like the tunnel FET to take us lower? What are the circuits and architectures challenges for low voltage digital systems?

  Panelists: I. Young (Intel), E. Alon (UC Berkeley), T. Skotnicki (STMicroelectronics), Y.-C. Yeo (National Univ. of Singapore), A. Toriumi (Univ. of Tokyo)

- "***Novel hierarchy in emerging memory",*** moderated by G. Bronner (Rambus) and N. Takaura (Low-power Electronics Association & Project (LEAP)), will debate on the scalability, speed, and power consumption of STT-MRAM, PCM, ReRAM and their strengths and weaknesses versus existing memories. Both the theoretical understanding and the practical tradeoffs needed to ramp these technologies in high volume manufacturing will be discussed.

  Panelists: S. Fujita (Toshiba, MRAM), P. G. Cappellitti (Micron, PCRAM), G. Jeong (Samsung, ReRAM), E-X. Ping (AMAT, material aspects), Yoon (IBM, DRAM/Flash), K. Shiraishi (Univ. of Tsukuba, Modeling)

The **Symposium on VLSI Circuits** also will hold two parallel rump sessions, on Thursday evening June 13, 2013.

- "***The Best Logic and Memory Interface Technology for 2D/2.5D/3D ICs",*** moderated by N. Lu (Etron) and K. Chang(Xilinx), will discuss the best interface technology for 2D, 2.5D, or 3D IC designs. The purpose of this panel is not to select the final champion among these emerging designs but to invite the world's top designers and technologists to present and to debate on the pros and cons of these interface designs.

  Panelists: F. Chang (UCLA), T. Kuroda (Keio Univ.), K. Matsudera (Toshiba), L. Madden (Xilinx), S. Pawlowski (Intel), T. Pawlowski (Micron), K. Sohn (Samsung), E. Tsern (Rambus)

- "***Analog designer's play-ground beyond 20nm, is it Circuit Physics or Auto Place&Route?",*** moderated by A. Cathelin (STMicroelectronics) and C.-M. Hung (MStar Semiconductor /MediaTek), will deal with following questions: How should the analog (non-digital) designers treat the design with 1Xnm transistor? Should we go to a pure "place and route" strategy over a gate-array matrix? Or, should we continue designing like in the "good old analog era"?

  Panelists: P. Dautriche (STMicroelectronics), G. Taylor (Intel), K. Okada (Tokyo Institute of Tech.), F.-L. Hsueh (TSMC), S. Masui (Fujitsu)

The organizers of the VLSI Technology rump sessions (C-P. Chang – Applied Materials and N. Sugii - LEAP) and of the VLSI Circuits rump sessions (J. DeBrosse – IBM, H. Noda – Elpida Memory, N. Lu – Etron, A. Cathelin – STMicroelectronics, and C.-M. Hung – MStar Semiconductor /MediaTek) invite all attendees of both VLSI Symposia to participate.

Joint Banquet

On Wednesday evening, June 12, 2013, a joint banquet will be held to provide an informal, relaxed atmosphere for information exchange between technologists and circuit designers.

Joint Luncheon (Separate registration required)

On Thursday, June 13, 2013, a luncheon sponsored by both Symposia will feature the talk "Symbiosis with Lightning which is one of the most spectacular natural phenomenon" by Dr. Takeshi Kudo, Otowa Electric, Japan. He will talk about the "Lightning" and its beautiful flash / thunderous roar generated by huge amounts of electric energy. He will present a lightning phenomena showing some sample photos and will present lighting arrester (Surge Protective Device) which support the social life. Also, he will introduce the basic method and equipment for lightning protection on electrical systems.

Short Courses (Separate registration required)

- **VLSI Technology Short Course (June 10)** -- ***"Technology Enablers for the Future Smart Society"*** -- This course will comprise six lectures given by distinguished speakers. A word "Smart" is exemplary of how our future society will be progressive with vast kinds of technological features, such as fast-logic computing, energy-saving, versatile connectivity, real-time information sharing, and various mobile-gears for network/cloud computing, supported by various technological elements of advanced logic and memory devices, efficient system chips, high-density packaging, and their fabrication methods, which will address topics of interest to both Technology and Circuits attendees.

  Invited speakers will be I. R. Post (Intel, Advanced CMOS device), C. H. Tung (TSMC, Advanced chip packaging), A. Chen (ASML, Advanced lithography and patterning), Y.Egawa (Toshiba, Advanced CMOS image sensor), T. Endo (Tohoku Univ., STT-MTJ Logic), and K. Sakui (Micron, New generation memories).

- **VLSI Circuits Short Courses (June 11)** -- Two parallel full-day courses will be given by 12 distinguished international speakers from industry and academia. A single registration fee covers both, and participants can freely switch between the two.

  - ***"Device-Aware Circuit Design in the Era of Disruptive Changes"***
    Invited speakers will be L. Seok-Hee (KAIST, CMOS technologies), K. Takeuchi (Renesas, Variability in MOS Transistors), D. Somasekhar (Intel, Digital Design), I. Fujimori (Broadcom, Wireline Transceivers), K. Imura (Maxlinear, Foundry Based IC Design), and P. Dautriche (STMicroelectronics, Device-Aware Design).

  - ***"Non-Volatility and 3D-Ability: Empowering LSI-based Smart Systems of Tomorrow"***
    Invited speakers will be K. Tsutsui (Sony, New NV Memories), K. Takeuchi (Chuo Univ., Solid-State Storage System), J. H. Yoon (IBM, Emerging Non-Volatile Memory), M. Koyanagi (Tohoku Univ., 3D Heterogeneous System Integration), J. T. Pawlowski (Micron, 3-D Integration), and L. Madden (Xilinx, 3-D Stacking).

Sponsoring Organizations

The VLSI Technology Symposium began in 1981, while the VLSI Circuits Symposium was added in 1987. The two meetings have been held together ever since, rotating annually between Japan and Hawaii. The Symposium on VLSI Technology is sponsored by the Japan Society of Applied Physics and the IEEE Electron Devices Society, in cooperation with the IEEE Solid State Circuits Society. The Symposium on VLSI Circuits is sponsored by the Japan Society of Applied Physics, the IEEE Solid-State Circuits Society, in cooperation with the Institute of Electronics, Information and Communication Engineers and the IEEE Electron Devices Society.

Further Information and Registration

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