SECOND ANNOUNCEMENT AND CALL FOR PAPERS

2015 SYMPOSIUM ON VLSI TECHNOLOGY

Sponsored by the Japan Society of Applied Physics and the IEEE Electron Devices Society
in cooperation with the IEEE Solid-State Circuits Society

Rihga Royal Hotel Kyoto, Kyoto, Japan
Monday - Thursday, June 15th – 18th, 2015
(June 15th Short Course, June 16th – 18th Technical Sessions)

www.vlsisymposium.org

The 2015 Symposium on VLSI Technology welcomes the submission of original papers on all aspects of IC technology. The 2015 Symposium on VLSI Circuits (please see the reverse side) will be held at the same location, with two days of overlap. **A single registration fee allows participants to attend both symposia** to facilitate synergistic interactions among participants in areas of joint interest.

SYMPOSIUM SCOPE

Symposium scope includes new concepts and breakthroughs in VLSI technology devices and processes including:

- Memory, Logic, RF, Analog, Mixed-Signal, I/O, High-Voltage, Imaging, MEMS, integrated sensors, and SOC (system-on-chip)
- Advanced gate stacks, channels, source/drain junctions and contacts
- Heterogeneous integration of non-Si materials/substrates on Si substrates
- Advanced lithography and high-density VLSI patterning technologies
- Beyond-CMOS functional devices with a path for VLSI implementation
- Interconnect scaling and Cu alternatives; chip-to-chip including optical interconnects
- Packaging technologies, through-silicon-vias (TSVs) and 3D-system integration
- Advanced materials, device analysis, and modeling
- Theoretical understanding, operation fundamentals and reliability issues related to the above devices
- VLSI manufacturing concepts, technologies and yield optimization

JOINT TECHNOLOGY AND CIRCUITS FOCUS SESSIONS

Joint technology and circuits focus sessions comprising invited and contributed papers will be offered in special areas. Paper submissions highlighting **major innovations and advances in materials, processes, devices, integration, reliability and modeling** are strongly encouraged in the following areas of joint interest:

- **Design in scaled technologies:** Impact of advanced devices, structures, materials and interconnects on digital circuit performance, power, density; device design & process/technology optimization for analog/mixed-signal circuits
- **Design enablement:** Technology and design co-optimization for improved performance, yield, reliability, ultra-low voltage/power operation, density, and cost
- **Memory technologies:** Discrete and embedded SRAM, DRAM and NVRAM (Flash, ReRAM, PCRAM, STT-MRAM, etc.) technology/design co-optimization
- **3D-integration (TSV):** 3D-technologies and system co-optimization; power delivery and management; thermal management; inter-chip communications.

SUBMISSION OF PAPERS

Prospective authors must upload their submission of a two-page camera-ready paper and a 150-word-abstract to www.vlsisymposium.org. Authors must follow detailed instructions provided within the "Authors" section of the website, including the Authors' Guide and Pre-publication Policy. The technical content beyond the 150-word-abstract of the accepted paper must not be announced, published, or in any way put in the public domain prior to the Symposium.

Paper Submission Deadline: 23:59 JST (14:59 GMT), Monday January 26th, 2015

BEST STUDENT PAPER AWARD

The student paper award selection will be based upon the quality of the paper and the presentation. The recipient will be presented a financial prize and a certificate at the opening session of the 2016 Symposium. For a paper to be reviewed for this award, the author must be enrolled as a full-time student at the time of submission, must be the lead author and presenter of the paper, and must indicate on the web submission form that the paper is a student paper.

LATE NEWS

Late news abstracts announcing very recent results with high impact are also invited. **Deadline for late news submissions is March 26th, 2015.** Note that only a very limited number of top quality late news papers will be accepted. Submission procedure will be announced on the 2015 VLSI Symposia website.

VLSI TECHNOLOGY SHORT COURSE

A one-day short course on topics of major interest will be offered on June 15th, 2015, instructed by leading subject matter experts. Details will be posted on the VLSI Technology Symposium website by the middle of April, 2015.

SATELLITE WORKSHOPS

The 2015 Silicon Nanoelectronics Workshop will be held on June 14th – 15th, 2015 as a satellite workshop at the same location. In addition, the 2015 Spintronics Workshop focusing on VLSI-implementable Spintronics Technology will be held on June 15th, 2015 also at the same location.

Secretariat for VLSI Symposia - Japan & Asia
c/o ICS Convention Design, Inc., Tokyo, Japan
Tel: +81-3-3219-3541
E-mail: vlsisymp[at]ics-inc.co.jp

Secretariat for VLSI Symposia - America & Europe
Widerkehr and Associates, Montgomery Village, MD, USA
Tel: +1-301-527-0900, extension 2
E-mail: vlsi[at]vlsisymposium.org