2016 Symposia on VLSI Technology and Circuits - Technology Short Course - June 13 Monday
Spintronics Workshop, June 13

SiNano Electronics Workshop - June 12 - 13 Sunday/Monday

2016 Symposia on VLSI Technology and Circuits June 14th - Tuesday

Time	Honolulu I	Honolulu II	Tapa I		Tapa II		Tapa III	
			Technology Plenary and Welcome					
8:05 AM				Welcome and Opening Remarks				
8:35 AM			InvenSense	The Age of Sensors – How MEMS sensors will enable the next wave of new products (Invited)				
9:20 AM			Nissan	Intelligent Mobility realized through VLSI (Invited)				
	Circ. SC	Circ. SC	T2: Technology Highlights Session					
10:25 AM	10:30 AM - 5:05 PM	10:30 AM - 5:05 PM	Samsung Elect.	Si FinFET based 10nm Technology with Multi Vt Gate Stack for Low Power and High Performance Applications				
10:50 AM			IBM	FINFET Technology Featuring High Mobility SiGe Channel for 10nm and Beyond				
11:15 AM			TSMC	High performance In0.53Ga0.47As FinFETs fabricated on 300 mm Si substrate				
11:40 AM			Headway Tech.	Achieving Sub-ns switching of STT-MRAM for future embedded LLC applications through improvement of nucleation and propagation switching mechanisms				
			T3: System and Embedded Memory		T4: Ge and SiGe Channel Devices		T5: Device Reliability	
1:30 PM			Micron	Memory: Welcome to the Era of Innovative Architectures (Invited)	Liverpool John Moores U.	Understanding charge traps for optimizing Si-passivated Ge nMOSFETs	imec	Demonstration of an InGaAs gate stack with sufficient PBTI reliability by thermal budget optimization, nitridation, high-k material choice, and interface dipole
1:55 PM			Toshiba Corp.	High-Density User-Programmable Logic Array Based on Adjacent Integration of Pure-CMOS Crossbar Antifuse into Logic CMOS Circuits	imec	A 2nd Generation of 14/16nm-node compatible strained-Ge pFINFET with improved performance with respect to advanced Si-channel FinFETs	GLOBAL-FOUNDRIES	Application of CVS and VRS method for correlation of logic CMOS wear out to discrete device degradation based on Ring Oscillator circuits
2:20 PM			Hitachi, Ltd.	Advanced Non-volatile Embedded Memories for a Wide Range of Applications (Invited)	IBM Research	Selective GeOx-Scavenging from Interfacial Layer on Si1-xGex Channel for High Mobility Si/Si1-xGex CMOS Application	Toshiba Corp.	Deep Insight into Process-induced Pre-existing Traps and PBTI Stress-induced Trap Generations in High-k Gate Dielectrics through Systematic RTN Characterizations and Ab initio Calculations
2:45 PM			Winbond Elec. Corp.	Random Soft Error Suppression by Stoichiometric Engineering: CMOS Compatible and Reliable 1Mb HfO2-ReRAM with 2 Extra Masks for Embedded IoT Systems	IBM	Demonstration of Record SiGe Transconductance and Short-Channel Current Drive in High-Ge-Content SiGe PMOS FinFETs with Improved Junction and Scaled EOT	CEA-LETI	Hot Carrier Degradation in Nanowire Transistors: Physical mechanisms, Width dependence and Impact of Self-Heating
			T6: Novel 2D Materials and Devices		T7: Contact Resistance Innovations for Sub-10nm Scaling		T8: High Density Non Volatile Memory	
3:25 PM			NARL	MoS2 U-shape pMOSFET with 10 nm Channel Length and Doped Poly-Si MoS2 U-shape pMOSFET with 10 nm Channel Length and Doped Poly-Si Source/Drain Serving as Seed for Full Wafer CVD MoS2 Availability	Katholieke U. Leuven	Ultralow-Resistivity CMOS Contact Scheme with Pre-Contact Amorphization Plus Ti (Germano-)Silicidation	Kookmin U.	Comprehensive evaluation of early retention (fast charge loss within a few seconds) characteristics in tube-type 3-D NAND Flash Memory
3:50 PM			MIT	Serially B7:B29Connected Monolayer MoS2 FETs with Channel Patterned by a 7.5 nm Resolution Directed Self-Assembly Lithography	IBM Research	Ti and NiPt/Ti Liner Silicide Contacts for Advanced Technologie	Macronix Int. Co., LTD.	A Monte Carlo Simulation Method to Predict Large-density NAND Product Memory Window from Small-array Test Element Group (TEG) Verified on a 3D NAND Flash Test Chip
4:15 PM			Stanford U.	GDOT: A Graphene-Based Nanofunction for Dot-Product Computation	Applied Materials	Ultra-Low NMOS Contact Resistivity Using a Novel Plasma-Based DSS Implant and Laser Anneal for Post 7 nm Nodes	imec	Advanced a-VMCO resistive switching memory through inner interface engineering with wide (>1e2) on/off window, tunable uA-range switching current and excellent variability
4:40 PM			UMC	Extremely Low Power C-Axis Aligned Crystalline In-Ga-Zn-O 60 nm Transistor Integrated with Industry 65 nm Si MOSFET for IoT Normally-Off CPU Application		WITHDRAWN	Chinese Acad. of Sciences	Fully CMOS Compatible 3D Vertical RRAM with Self-aligned Self-selective Cell Enabling Sub-5nm Scaling
5:05 PM			Tohoku U.	A sub-ns three-terminal spin-orbit torque induced switching device	UMC	Ultra low p-type SiGe contact resistance FinFETs with Ti silicide liner using cryogenic contact implantation amorphization and Solid-Phase Epitaxial Regrowth (SPER)	POSTECH	Te-Based Amorphous Binary OTS Device with Excellent Selector Characteristics for X-point Memory Applications
5:30 PM			CEA-LETI	Si CMOS Platform for Quantum Information Processing				
7:15 PM			Joint Technology/Circuits Reception Tapa Conference Center, Palace Lounge					
8:00 PM			Technology Panel Session - Tapa I How Moore's Law, Industry Consolidation, and System Trends are Shaping the Memory Roadmap?		Joint Technology/Circuits Panel Session - Tapa II More Moore, More than Moore, or Mo(o)re Slowly?			

Color code
Technology (blue)
Circuits (red)
Joint Technology / Circuits (green)

2016 Symposia on VLSI Technology and Circuits June 15th - Wednesday

Time	Tapa I		Tapa II		Tapa III		Honolulu	
			Circuits Plenary and Welcome					
8:05 AM				Welcome and Opening Remarks				
8:35 AM			Google Inc.	Enabling Progress in Machine Learning (Invited)				
9:20 AM			SONY	Accelerating the Sensing World through Imaging Evolution (Invited)				
	C2: Memory Design		T9: Technology Scaling Beyond 10 nm		TJF10: Technology/Circuits Joint Focus Session:		C3: Oversampling Data Converters	
10:15 AM	TSMC	A 16nm Dual-Port SRAM with Partial Suppressed Word line, Dummy Read Recovery and Negative Bit-line Circuitries for Low VMIN Applications	TSMC	Demonstration of a sub-0.03 um2 High Density 6-T SRAM with Scaled Bulk FinFETs for Mobile SOC Applications Beyond 10nm Node	Texas Instr.	Smart Power Technologies Enabling Power SOC and SIP (Invited	Panasonic Corp.	A 97.99 dB SNDR, 2 kHz BW, 37.1 uW Noise-Shaping SAR ADC with Dynamic Element Matching and Modulation Dither
10:40 AM	Renesas Elec. Corp.	A 6.05-Mb/mm2 16-nm FinFET Double Pumping 1W1R 2-port SRAM with 313 ps Read Access	IBM Research GmbH	First Demonstration of InGaAs/SiGe CMOS Inverters and Dense SRAM Arrays on Si Using	Renesas Electronics	A Dynamic/Static SRAM Power Management Schemes for DVFS and AVS in Automotive	Oregon State U.	A 35µW 96.8dB SNDR 1 kHz BW Multi-Step Incremental ADC Using Multi-Slope
11:05 AM	NEC Corp.	A 2x Logic Density Programmable Logic Array using Atom Switch Fully Implemented with Logic Transistors at 40nm-node and beyond	IBM	Replacement High-K/Metal-Gate High-Ge-Content Strained SiGe FinFETs with High Hole Mobility and Excellent SS and Reliability at	HKUST	A Multiple-String Hybrid LED Driver with 97% Power Efficiency and 0.996 Power Factor	The U. of TX at Austin	A 18.5-fJ/step VCO-Based 0-1 MASH Delta-Sigma ADC with Digital Background Calibration
11:30 AM	GLOBAL-FOUNDRIES INDIA	80Kb 10ns Read Cycle Logic Embedded High-K Charge Trap Multi-Time-Programmable Memory Scalable to 14nm FIN with no Added Process	imec	Zero-thickness Multi Work Function Solutions for N7 bulk FinFETs	KAIST	A Sine-Reference Band (SRB)-Controlled Average Current Technique for a Phase-Cut Dimmable AC-DC Buck LED Driver without an	IIT Madras	A 13.3mW 60MHz Bandwidth, 76dB DR 6GS/s CTΔΣM with Time Interleaved FIR Feedback
	C4: Biomedical SOCs		TJF11: Analog / RF Integration and DTCO in CMOS		T12: Emerging Memory Technology (RRAM and PCM)		C5: Ultra High Speed Wireline Transceivers	
1:15 PM	Nanyang Tech U.	A 128-Channel Spike Sorting Processor Featuring 0.175 µW and 0.0033 mm2 per Channe	GLOBAL-FOUNDRIES	Overcoming Scaling Barriers through Design Technology CoOptimization (Invited)	Liverpool John Moores	RTN-based defect tracking technique: experimentally probing the spatial and energy	Xilinx	A Fully-Adaptive Wideband 0.5-32.75Gb/s FPGA Transceiver in 16nm
1:40 PM	Columbia Univ.	1.74-µW/ch, 95.3%-Accurate Spike-Sorting Hardware based on Bayesian Decision	TSMC	Analog/RF Wonderland: Circuits and Technology Co-optimization in Advanced FinFET Technology (Invited)	NEC Corp.	Robust Cu Atom Switch with over-400oC thermally tolerant Polymer-solid Electrolyte (TT-PSE) for Nonvolatile Programmable Logic	Socionext Inc.	A 28.3 Gb/s 7.3 pJ/bit 35 dB Backplane Transceiver with Eye Sampling Phase Adaptation in 28 nm CMOS
2:05 PM	Georgia Inst. of Tech.	A High-Density CMOS Multi-Modality Joint Sensor/Stimulator Array with 1024 Pixels for Holistic Real-Time Cellular Characterization	U. of Texas at Dallas	200-280GHz CMOS RF Front-End of Transmitter for Rotational Spectroscopy	imec	Retention, disturb and variability improvements enabled by local chemical-potential tuning and controlled Hour-Glass filament shape in a novel	Korea Univ.	A 32 Gb/s Rx Only Equalization Transceiver with 1-tap Speculative FIR and 2-tap Direct IIR DFE
2:30 PM	Delft Univ. of Techn.	A Front-end ASIC with Receive Sub-Array Beamforming Integrated with a 32 × 32 PZT Matrix Transducer for 3-D Transesophageal	Rice U.	Broadband THz Spectroscopic Imaging based on a Fully Integrated 4×2 Digital-to-Impulse Radiating Array with a Full-Spectrum of	Macronix	A Novel Low Power Phase Change Memory Using Inter-Granular Switching	Xilinx Inc	A 56Gb/s PAM4 Wireline Transceiver using a 32-way Time-Interleaved SAR ADC in 16nm FinFET
	C6: Voltage Regulation		T13: FDSOI and III-V Devices		T14: FDSOI and III-V Devices		C7: Low Power RF-Transceivers	
2:55 PM	HKUST	A 50MHz 5V 3W 90% Efficiency 3-Level Buck Converter with Real-Time Calibration and Wide Output Range for Fast-DVS in 65nm CMOS	CEA LETI	Smart Solutions for Efficient Dual Strain Integration for Future FDSOI Generations	TSMC	Reliability study of perpendicular STT-MRAM as emerging embedded memory qualified for reflow soldering at 260oC	TSMC	A Bluetooth Low-Energy (BLE) Transceiver with TX/RX Switchable On-Chip Matching Network, 2.75mW High-IF
3:20 PM	Nat'l Chiao Tung Univ.	95% Light-load Efficiency Single-Inductor Dual-Output DC-DC Buck Converter with Synthesized Waveform Control Technique for USB Type-C	CEA-LETI	High Performance CMOS FDSOI Devices activated at Low Temperature	Toshiba Corp.	Sub-3 ns pulse with sub-100 uA switching of 1x-2x nm perpendicular MTJ for high-performance embedded STT-MRAM towards sub-20 nm	U. of Michigan	A 380pW Dual Mode Optical Wake-up Receiver with Ambient Noise Cancellation
3:45 PM	KAIST	A Reconfigurable SIMO System with 10-Output Dual-Bus DC-DC Converter using the Load Balancing Function in Group Allocator for	MIT	High aspect ratio InGaAs FinFETs with sub-20 nm fin width	Toshiba Corp.	First demonstration and performance improvement of ferroelectric HfO2-based resistive switch with low operation current	U. Catholique de Louvain	SleepTalker: a 28nm FDSOI ULV 802.15.4a IR-UWB Transmitter SoC achieving 14pJ/bit at 27Mb/s with Adaptive-FBB
4:10 PM	NXP Semiconductors	A Microcontroller with 96% Power-Conversion Efficiency using Stacked Voltage Domains	Imec	Junctionless Gate-All-Around Lateral and Vertical Nanowire FETs with Simplified Processing for	National Chiao-Tung U.	One-Transistor Ferroelectric Versatile Memory:Strained-Gate Engineering for Realizing	KAIST	A 2.4GHz Ternary Sequence Spread Spectrum OOK Transceiver with Harmonic Spur Suppression and Dual-Mode
4:35 PM	STMicroelectronics	A Fast, Flexible, Positive and Negative Adaptive Body-Bias Generator in 28nm FDSOI	IMEC/KULeuven	Record mobility (µeff ~3100 cm2/V-s) and reliability performance (Vov~0.5V for 10yr	The U. of Tokyo	Study of wake-up and fatigue properties in doped and undoped ferroelectric HfO2 in	Toshiba Corp.	An 18 µW Spur Canceled Clock Generator for Recovering Receiver Sensitivity in
5:20 PM	Executive Panel - Semiconductor Business: Inflections Beyond Scaling 5:20 PM - 6:50 PM, Mid-Pacific Conference Center, Coral IV & V							
7:00 PM	Banquet							

2016 Symposia on VLSI Technology and Circuits June 16th - Thursday

Time	Tapa I		Tapa II		Tapa III		Honolulu	
	C8: Circuits Focus Session: Innovative Systems for a Smart Society		T15: Gate All Around and III-V Devices		T16: Variability and Design Technology Co-Optimization		C9: Power Management	
8:05 AM	Intel Corp.	An Energy Harvesting Wireless Sensor Node for IoT Systems Featuring a Near-Threshold Voltage IA-32 Microcontroller in 14nm	imec	Gate-All-Around MOSFETs based on Vertically Stacked Horizontal Si Nanowires in a Replacement Metal Gate Process on Bulk	Purdue Univ.	RTN and Low Frequency Noise on Ultra-scaled Near-ballistic Ge Nanowire nMOSFETs	U. of Michigan, Ann Arbor	A 66pW Discontinuous Switch-Capacitor Energy Harvester for Self-Sustaining Sensor Applications
8:30 AM	Rambus	Lensless Smart Sensors: Optical and Thermal Sensing for the Internet of Things (Invited Paper)	TSMC Europe	InAs Nanowire GAA n-MOSFETs with 12-15 nm Diameter	Stanford U.	Statistical Limits of Contact Resistivity Due to Atomistic Variation in Nanoscale Contacts	Keio U.	A Wireless Power Transfer System with Enhanced Response and Efficiency by Fully-Integrated
8:55 AM	NIDEK Co. Ltd.	Features of retinal prosthesis using suprachoroidal transretinal stimulation from an electrical circuit perspective (Invited Paper)	Lund U.	InGaAs Nanowire MOSFETs with ION = 555 µA/µm at IOFF = 100 nA/µm and VDD = 0.5 V	Peking U.	Variability-aware TCAD Based Design-Technology Co-Optimization Platform for	U. of California, San Diego	A Fully Integrated 144 MHz Wireless-Power-Receiver-on-Chip
9:20 AM	Texas Instr.	Multi-modal Smart Bio-sensing SoC Platform with >80dB SNR 35µA PPG RX Chain	KU Leuven	Top-down InGaAs Nanowire and Fin Vertical FETs with Record Performance	Intel Corp.	Random Telegraph Noise (RTN) in 14nm Logic Technology: High Volume	Delft U. of Tech.	A ±36A Integrated Current-Sensing System with 0.3% Gain Error and
9:45 AM	Fujitsu	An FPGA-accelerated Partial Image Matching Engine for Massive Media Data Searching Systems (Invited Paper)	IMEC	Scalability of InGaAs Gate-All-Around FET integrated on 300mm Si platform: Demonstration of channel width	STMicroelectronics	Design / technology co-optimization of strain-induced layout effects in 14nm UTBB-FDSOI CMOS: enablement and assessment	U. of Michigan, Ann Arbor	A 114-pW PMOS-Only, Trim-Free Voltage Reference with 0.26%
	C10: Circuits Focus Session: Industrial and Power Circuit Directions for a Smart Society		T17: Technology Focus Session: Interconnect and 3D Integration		T18: Non Volatile Memories and Applications		C11: RF Transceiver Techniques	
10:25 AM	Texas Instr.	Motor Control Used to Be Boring (Invited Paper)	IMEC	On-chip Interconnect Trends, Challenges and Solutions: How to Keep RC and Reliability Under Control (Invited)	imec	Direct three-dimensional observation of the conduction in poly-Si and In1 xGaxAs 3D NAND vertical channels	UC Berkeley	A 65nm CMOS Transceiver with Integrated Active Cancellation Supporting FDD from 1GHz
10:50 AM	Panasonic Corp.	A Fully Integrated GaN-based Power IC Including Gate Drivers for High-Efficiency DC-DC Converters (Invited Paper)	Tokyo Inst. Of Tech.	Production-Worthy WOW 3D Integration Technology using Bumpless Interconnects and Ultra-Thinning Processes (Invited)	Stanford U.	Four-Layer 3D Vertical RRAM Integrated with FinFET as a Versatile Computing Unit for Brain-Inspired Cognitive	UCLA	Digital PLL for Phase Noise Cancellation in Ring Oscillator-Based I/Q Receivers
11:15 AM	Analog Devices Inc	A Transformer-based Digital Isolator With 20kVPK Surge Capability and > 200k	CEA, Leti, MINATE	First demonstration of a CMOS over CMOS 3D VLSI CoolCube integration on 300mm	Pol. di Milano	Novel RRAM-enabled 1T1R synapse capable of low-power STDP via burst	Columbia U.	A Chopping Switched-Capacitor RF Receiver with Integrated
11:40 AM	STMicroelectronics	Innovative System on Chip Platform for Smart Grids and Internet of Energy Applications (Invited Paper)	National Tsing Hua U.	A Highly Scalable Poly-Si Junctionless FETs Featuring a Novel Multi-Stacking Hybrid P/N Layer and Vertical Gate with Very	Panasonic Semi. Solutions Corp.	A ReRAM-based Physically Unclonable Function with Bit Error Rate < 0.5% after 10 years at 125˚C for 40nm Embedded	Broadcom	A 180 mW Multistandard TV Tuner in 28 nm CMOS
12:15 PM	Luncheon Talk Cyborg Insects and Other Things: Building Interfaces Between the Synthetic and the Multicellular Michel Maharbiz, University of California, Berkeley 12:15 PM - 1:30 PM, Mid-Pacific Conference Center, Nautilus Suite							
	CJF12: Circuit/Technology Joint Focus Session: Embedded Memories		T19: High-K Metal Gate Variability and Scaling		T20: Sensor Technology and Microsystems for IoT		C13: Analog Techniques	
1:30 PM	POSTECH	Full Chip Integration of 3-D Cross-Point ReRAM with Leakage-Compensating Write Driver and Disturbance-Aware Sense Amplifier	CEA-LETI	Gate Stack Solutions in Gate-First FDSOI Technology to meet High Performance, Low Leakage, VT centering and Reliability Criteria	Carnegie Mellon U.	Low-Power, High-Performance S-NDR Oscillators for Stereo (3D) Vision using Directly-Coupled Oscillator Networks	Oregon State U.	A 0.6mW 31MHz 4th-Order Low-Pass Filter with +29dBm IIP3 Using Self-Coupled Source Follower
1:55 PM	Semi. Energy Lab	Embedded Memory and ARM Cortex-M0 Core Using 60 nm C-Axis Aligned Crystalline Indium–Gallium–Zinc Oxide FET Integrated	National Chiao Tung U.	A New Variation Plot to Examine the Interfacial-dipole Induced Work-function Variation in Advanced High-k Metal-gate CMOS Devices	U. of Notre Dame	Ultra Low Power Coupled Oscillator Arrays for Computer Vision Applications	Technische U. Dresden	3.5mW 1MHz AM Detector and Digitally-Controlled Tuner in a-IGZO TFT for
2:20 PM	Chuo U.	Versatile TLC NAND Flash Memory Control to Reduce Read Disturb Errors by 85% and Extend Read Cycles by 6.7-times	GLOBAL FOUNDRIES	Novel N/PFET Vt control by TiN Plasma Nitridation for Aggressive Gate Scaling	Nanyang Tech. U.	A 512×576 65-nm CMOS ISFET Sensor for Food Safety Screening with 123.8 mV/pH Sensitivity and 0.01 pH Resolution	U. of Michigan, Ann Arbor, MI	A 16-channel Noise-Shaping Machine Learning Analog-Digital Interface
2:45 PM	Intel Corp.	A 0.9um2 1T1R Bit Cell in 14nm SoC Process for Metal-Fuse OTP Array with Hierarchical Bitline, Bit Level Redundancy,	TU Wien	Complete Extraction of Defect Bands Responsible for Instabilities in n and pFinFETs	National Chiao Tung U.	Integration of Neural Sensing Microsystem with TSV-embedded Dissolvable µ-Needles Array, Biocompatible Flexible	Seoul National U.	A Field-Programmable Mixed-Signal IC with Time-Domain Configurable Analog Blocks
	CJF14: Circuits/Technology Joint Focus Session: Design in Scaled Technologies		T21: Steep Sub-Threshold Devices		T22: CMOS Image Sensors		C15: Successive Approximation ADCs	
3:25 PM	UC,Davis	A 5.8 pJ/Op 115 Billion Ops/sec, to 1.78 Trillion Ops/sec 32nm 1000-Processor Array	Intel Corp.	Enabling High-Performance Heterogeneous TFET/CMOS Logic with Novel Circuits Using TFET Unidirectionality and	Renesas Electronics Corp.	White Spots Reduction by Ultimate Proximity Metal Gettering at Carbon Complexes Formed	U. of Southern California	A 12-bit 1.6 GS/s Interleaved SAR ADC with Dual Reference Shifting and Interpolatio
3:50 PM	ST Microelectronics	28nm FDSOI Technology Sub-0.6V SRAM Vmin Assessment for Ultra Low Voltage Applications	The U. of Tokyo	Performance improvement of InxGa1-xAs Tunnel FETs with Quantum Well and EOT scaling	National Nano Device Labs.	Enabling monolithic 3D image sensor using large-area monolayer transition metal dichalcogenide and logic/memory hybrid	MediaTek Inc.	A 14.6mW 12b 800MS/s 4×Time-Interleaved Pipelined SAR ADC achieving 60.8dB SNDR
4:15 PM	ARM Research	A 400mV Active VMIN, 200mV Retention VMIN, 2.8 GHz 64Kb SRAM with a 0.09 um2 6T bitcell in a 16nm FinFET CMOS Process	IBM Research - Zurich	Complementary III-V Heterojunction Lateral NW Tunnel FET Technology on Si	National U. of Singapore	Germanium-Tin Heterojunction Phototransistor: Towards High-Efficiency Low-Power Photodetection in	Korea U.	An Oscillator Collapse-Based Comparator with Application in a 74.1dB SNDR, 20kS/s 15b
4:40 PM	Intel Corp.	A 350mV-900mV 2.1GHz 0.011mm2 Regular Expression Matching Accelerator with Aging-Tolerant Low-VMIN	Penn State	Monolithic Phase-transition-FET Exhibiting Steep Switching Slope of 8mV/decade and 36% Enhanced ON Current	TowerJazz	Novel Pixel Structure with Stacked Deep Photodiode to Achieve High NIR Sensitivity and High MTF	National Tsing Hua U.	A 0.44fJ/conversion-step 11b 600KS/s SAR ADC with Semi-Resting DAC
5:05 PM	Qualcomm	Unified Technology Optimization Platform using Integrated Analysis (UTOPIA) for holistic technology, design and system	UC,Berkeley	Circuit Performance Analysis of Negative Capacitance FinFETs	U. of Edinburgh	Back-illuminated voltage-domain global shutter CMOS image sensor with 3.75µm pixels and dual in-pixel storage nodes		
5:45 PM	IEEE Solid-States Circuits Society Young Professionals and Grad Students Mentoring and Career coaching event Honolulu Suites Lanai - Thursday, June 16, 5:45 PM – 6:45 PM							
8:00 PM	Circuits Panel Session - Tapa I Top circuit techniques: Life with and without them		Circuits Panel Session - Tapa II It's all a common platform – how do I build a differentiated product?					

2016 Symposia on VLSI Technology and Circuits June 17th - Friday

Time	Tapa I		Tapa II		Tapa III	
	C16: Advanced Wireline Techniques		C17: Digital Architectures and Processors		C18: Advanced Sensor Circuits	
8:05 AM	U. of Alberta	A 35 mW 10 Gb/s ADC-DSP less Direct Digital Sequence Detector and Equalizer in 65nm CMOS	KU Leuven	A 0.3-2.6 TOPS/W Precision-Scalable Processor for Real-Time Large-Scale ConvNets	N. U. of Science and Tech.	A 0.23 micro-g Bias Instability and 1.6 micro-g/rt(Hz) Resolution Silicon Oscillating Accelerometer with Build-in Sigma-Delta Frequency-to-Digital Converter
8:30 AM	Broadcom Corp	A 125 mW 8.5-11.5 Gb/s Serial Link Transceiver with a Dual Path 6-bit ADC/5-tap DFE Receiver and a 4-tap FFE Transmitter in 28 nm CMOS	U. of Michigan	A 1.40mm2 141mW 898GOPS Sparse Neuromorphic Processor in 40nm CMOS	Delft U. of Tech.	A BJT-based Temperature-to-Digital Converter with ±60mK (3σ) Inaccuracy from -70°C to 125°C in 160nm CMOS
8:55 AM	Stanford U.	A 0.003 mm² 5.2 mW/tap 20 GBd Inductor-less 5-Tap Analog RX-FFE	UCLA	A 190GFLOPS/W DSP for Energy-Efficient Sparse-BLAS in Embedded IoT	Intel Germany	A 28nm CMOS Ultra-Compact Thermal Sensor in Current-Mode Technique
9:20 AM	UCLA	A 16Gb/s 14.7mW Tri-Band Cognitive Serial Link Transmitter with Forwarded Clock to Enable PAM-16/256-QAM and Channel Response Detection in 28 nm CMOS	MIT	A 58.6mW Real-Time Programmable Object Detector with Multi-Scale Multi-Object Support Using Deformable Parts Model on 1920x1080 Video at 30fps	KAUST	A 35fJ/Step Differential Successive Approximation Capacitive Sensor Readout Circuit with Quasi-Dynamic Operation
9:45 AM	POSTECH	A Low-EMI Four-Bit Four-Wire Single-Ended DRAM Interface by Using a Three-Level Balanced Coding Scheme	Intel Corp.	Adaptive Clocking with Dynamic Power Gating for Energy Efficiency Improvement in a 22nm Graphics Execution Core under Fast Voltage Droop	Nanyang Tech. U.	A 9.84–73.2 nJ, 0.048 mm2 Time-Domain Impedance Sensor that Provides Values of Resistance and Capacitance
	C19: High Speed Data Converters		C20: VCOs and Optical Building Blocks		C21: Advanced Imagers	
10:25 AM	U. of Texas at Dallas	A 23mW 24GS/s 6b Time-Interleaved Hybrid Two-Step ADC in 28nm CMOS	Xilinx Inc.	A 7-to-18.3GHz Compact Transformer based VCO in 16nm FinFET	Sony	An 8.3M-pixel 480fps Global-Shutter CMOS Image Sensor with Gain-Adaptive Column ADCs and 2-on-1 Stacked Device Structure
10:50 AM	MediaTek Inc.	A 8.2-mW 10-b 1.6-GS/s 4× TI SAR ADC with Fast Reference Charge Neutralization and Background Timing-Skew Calibration in 16-nm CMOS	U. of Texas at Dallas	-197dBc/Hz FOM 4.3-GHz VCO Using an Addressable Array of Minimum-Sized NMOS Cross-Coupled Transistor Pairs in 65-nm CMOS	Tohoku U.	A Dead-time Free Global Shutter CMOS Image Sensor with in-pixel LOFIC and ADC using Pixel-wise Connections
11:15 AM	Analog Devices	A 14-bit 2.5GS/s and 5GS/s RF Sampling ADC with Background Calibration and Dither	Oracle Labs	A 10Gb/s, 342fJ/bit Micro-Ring Modulator Transmitter with Switched-Capacitor Pre-Emphasis and Monolithic Temperature Sensor in 65nm CMOS	Stanford U.	A 220pJ/Pixel/Frame CMOS Image Sensor with Partial Settling Readout Architecture
11:40 AM	Texas Instr.	A 14-bit 8.9GS/s RF DAC in 40nm CMOS achieving >71dBc LTE ACPR at 2.9GHz	Hitachi Ltd.	A 50.6-Gb/s 7.8-mW/Gb/s –7.4-dBm Sensitivity Optical Receiver based on 0.18-um SiGe BiCMOS Technology	U. of Michigan	A 260µW Infrared Gesture Recognition System-on-Chip for Smart Devices
12:15 PM	IEEE Solid-State Circuits Society Luncheon 30th Symposium on VLSI Circuits 12:15 PM - 1:30 PM, Tapa Conference Center, Honolulu Suite					
	C22: Clock and Frequency Synthesis		C23: Hardware Security and Application Specific Digital Design		C24: Neural Interfaces and Processing	
1:30 PM	KHUST	An Inductor-less Fractional-N Injection-Locked PLL with a Spur-and-Phase-Noise Filtering Technique	Intel Corp.	250mV-950mV 1.1Tbps/W Double Affine Mapped Sbox based Composite-Field SMS4 Encrypt/Decrypt Accelerator in 14nm Tri-gate CMOS	Caltech	A 16-Channel 1.1mm2 Implantable Seizure Control SoC with Sub-µW/Channel Consumption and Closed-Loop Stimulation in 0.18µm CMOS
1:55 PM	Tokyo Inst. of Tech.	An 8.865-GHz -244dB-FOM High-Frequency Piezoelectric Resonator-Based Cascaded Fractional-N PLL with Sub-ppb-Order Channel Adjusting Technique	U. of Michigan	A Compact 446 Gbps/W AES accelerator for Mobile SoC and IoT in 40nm	RIKEN	A Microelectrode Array with 8,640 Electrodes Enabling Simultaneous Full-frame Readout at 6.5 kfps and 112-Channel Switch-Matrix Readout at 20 kS/s
2:20 PM	UCLA	A 2.4-GHz 6.4-mW Fractional-N Inductorless RF Synthesizer	Intel Corp.	A 4fJ/bit Delay-Hardened Physically Unclonable Function Circuit with Selective Bit Destabilization in 14nm Tri-gate CMOS	Aarhus U.	A Wearable Ear-EEG Recording System Based on Dry-Contact Active Electrodes
2:45 PM	Ulsan Nat'l Inst. of Science and Tech.	A PVT-Robust −59-dBc Reference Spur and 450-fsRMS Jitter Injection-Locked Clock Multiplier Using a Voltage-Domain Period-Calibrating Loop	U. of Michigan	A 0.58mm2 2.76Gb/s 79.8pJ/b 256-QAM Massive MIMO Message-Passing Detector	KAIST	A 2.048 Mb/s Full-Duplex Free-Space Optical Transceiver IC for a Real-Time In Vivo Neurofeedback Mouse Experiment Under Social Interaction
3:10 PM	TSMC	A 0.034mm2 , 725fs RMS Jitter, 1.8%/V Frequency-Pushing, 10.8-19.3GHz Transformer-Based Fractional-N All-Digital PLL in 10nm FinFET CMOS	Princeton U.	A Machine-learning Classifier Implemented in a Standard 6T SRAM Array	Columbia U.	A 450mV Timing-Margin-Free Waveform Sorter based on Body Swapping Error Correction