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Boosting Wireline Data Rates Beyond 56GB/s; Advanced Processors & Memory Structures Are Critical for the Next Generation of Connected Computing Systems

Two short courses at 2016 Symposia on VLSI Technology & Circuits examine design implications for high speed wireline transmission, and FinFET, FD-SOI & advanced memory technologies…

HONOLULU, HI (MAY 9, 2016) – Realizing the potential benefits of a connected society will require expanding the bandwidth of networked data systems, as well as developing new circuit designs leveraging the most advanced technologies to satisfy the challenging computational and memory requirements to process this data. To accomplish this, two full-day short courses are scheduled for June 14 in advance of the 2016 Symposia on VLSI Technology & Circuits. Presented by leading industry and academic experts the courses will address: ***"Advanced Wirelines Techniques"*** and ***"Circuit Design in FinFET, FD-SOI & Advanced Memory Technologies."***

Part of the Symposia's overall theme **"Inflections for a Smart Society,"** the two short courses address the challenges inherent in adapting advanced integration technologies for the IoT (Internet of Things) connected society.

The two full-day short courses are held in parallel sessions, with participants permitted to move between the two programs.

Course 1 – Advanced Wirelines Techniques

- *28 – 56GB/s Standards & Design Implications*, by Frank O'Mahony, Intel
- *Low Power CMOS Transceivers for 28Gb/s Serial Links & Future Prospects*, by Mounir Meghelli, IBM
- *ADCs for PAM-X / QAM-X Backplane & Optical Data Links*, by Aaron Buchwald, InPhi
- *56Gb/s Analog-based NRZ Electrical Transceiver*, by Hisakatsu Yamaguchi, Fujitsu Laboratory
- *Silicon Photonic Transceivers for Short-Reach Optical Interconnects*, by Joris Van Campenhout, imec
- *Integrated Electronic-Photonic Communication Circuits*, by Vladimir Stojanic, UC Berkely

Course 2 – Circuit Design in FinFET, FD-SOI & Advanced Memory Technologies

- *How the FinFET is Changing Processor Design*, by Jim Dodrill, ARM
- *Migrating Analog/Mixed-Signal Designs to FinFET*, by Alvin Loke, Qualcomm

• *Embedded Memory Design in CMOS FinFET Technology*, by Yih Wang, Intel
• *High Performance & High Reliability 3D Vertical NAND Flash*, by Woopyo Jeong, Samsung
• *SRAM & Digital Logic in UTTB FD-SOI*, by Bora Nikolic, UC Berkeley
• *FD-SOI Technology, Advantages for Analog/RF & Mixed-Signal Devices*, by Andreia Cathelin, STMicroelectronics

Separate registration is required for short course participation. Complete information about the program is available here: http://vlsisymposium.org/vlsi-circuits/

The 2016 Symposia on VLSI Technology & Circuits will be held at the Hilton Hawaiian Village, Honolulu, Hawaii from June 13-16, 2016 (Technology) and June 15-17, 2016 (Circuits). Held together since 1987, the Symposia provide a unique opportunity for the world's top device technologists, circuit and system designers to exchange leading edge research on microelectronics technology, with alternating venues between Hawaii and Japan.

Sponsoring Organizations
The Symposium on VLSI Technology is sponsored by the IEEE Electron Devices Society and the Japan Society of Applied Physics, in cooperation with the IEEE Solid State Circuits Society.

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Further Information, Registration and Program Details
Visit: http://www.vlsisymposium.org.
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