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Which Way Forward For Semi Integration:
"More Moore, More than Moore, or Mo(o)re Slowly?"

Panel discussion at 2016 Symposia on VLSI Technology & Circuits examines the industry's future direction as scaling slows down…

HONOLULU, HI (APRIL 5, 2016) – Underlying the semiconductor industry's soul-searching for a direction as the era of Moore's Law (geometric scaling) comes closer to its endpoint is the fundamental question: "What comes next?" Industry experts will examine possible answers in a joint panel session at the 2016 Symposia on VLSI Technology & Circuits, a premiere international conference on semiconductor technology that defines the pace, progress and evolution of microelectronics, scheduled from June 13-17, 2016 in Honolulu, Hawaii.

The joint panel session is part of the Symposia's overall theme **"Inflections for a Smart Society,"** reflecting the semiconductor industry's transition point as the pace of scaling slows and heterogeneous integration technologies rise to meet the challenges of an increasingly connected society (Internet of Things). Distinguished Chancellor's Professor Dr. Subramanian Iyer of UCLA's Electrical Engineering Department will moderate a panel of industry experts from the technology & circuits fields, including:

- Fari Assadaraghi, senior VP & CTO, NXP Semiconductors
- Vivek De, Intel Fellow & director of Circuit Technology Research, Intel
- Nicky Lu, Chairman & CEO, Etron Technology
- Gary Patton, CTO & senior VP of worldwide R&D, GLOBALFOUNDRIES
- Thomas Skotnicki, STM Fellow & director of advanced devices, STMicroelectronics
- Jan Vardaman, President, TechSearch International

"As the progression of geometric scaling slowing down, the industry faces an inflection point in the path toward technology innovation driving our increasingly connected society," said Dr. Malgorzata Jurczak, evening panel chair. "Does slower progress in scaling mean that large scale integration and its benefits will also slow down, or is it a blessing in disguise for new and innovative approaches at the circuit level? Our high profile panel will address these fundamental questions for the future."

"Moore's Law has many dimensions. Semiconductor technologists have followed 'the law,' shrinking silicon geometries by a factor of a million in last five decades. The challenge is now for our colleagues in system architecture, circuit design and packaging – and yes, let's not forget software – to follow suit. Miracles don't happen too often nowadays," stressed moderator Professor Iyer.

More information about the joint panel session is available here:
http://vlsisymposium.org/plenary-rump-sessions/#joint-panel-session

The annual Symposia on VLSI Technology & Circuits have made this industry transition its focal point, with the conference theme serving as the thread connecting the program elements. This year, the annual Symposia will be held at the Hilton Hawaiian Village, Honolulu, Hawaii from June 13-16, 2016 (Technology) and June 15-17, 2016 (Circuits). Held together since 1987, the Symposia provide a unique opportunity for the world's top device technologists, circuit and system designers to exchange leading edge research on microelectronics technology, with alternating venues between Hawaii and Japan.

Sponsoring Organizations
The Symposium on VLSI Technology is sponsored by the IEEE Electron Devices Society and the Japan Society of Applied Physics, in cooperation with the IEEE Solid State Circuits Society.

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Further Information, Registration and Program Details
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