FOR IMMEDIATE RELEASE – 20 APRIL, 2016

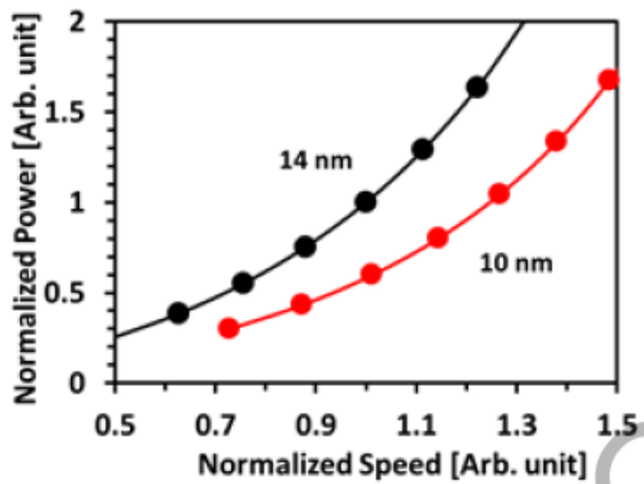
I) Technical Highlights from the Symposium on VLSI Technology

The 2016 Symposium on VLSI Technology is part of a premiere international conference that defines the pace, progress and evolution of microelectronics, scheduled from June 13-16, 2016 in Honolulu, Hawaii and held in conjunction with the Symposium on VLSI Circuits (June 14-17, 2016). The Symposia's overall theme "Inflections for a Smart Society," reflects the industry's transition point as "smart" system level applications help to transform the industry. Following are some of the highlighted papers that address this theme:

A) Semiconductor Technology Platform Papers for 10nm and Beyond

Samsung Electronics will present a 10nm logic technology developed using 3rd generation Si FinFETs for low power, high performance applications, demonstrating a speed improvement of 27% with a 40% reduction in power compared to 14nm process, achieved with multi-threshold voltage devices and reduced contact resistance.

Overcoming process challenges such as multiple patterning, high aspect ratio etching, niche gate replacements, and advanced isolation, the authors demonstrated yield analysis of a 0.04μm^2 SRAM with 128Mb cell size and observed a static noise margin of 190mV at 0.75V.

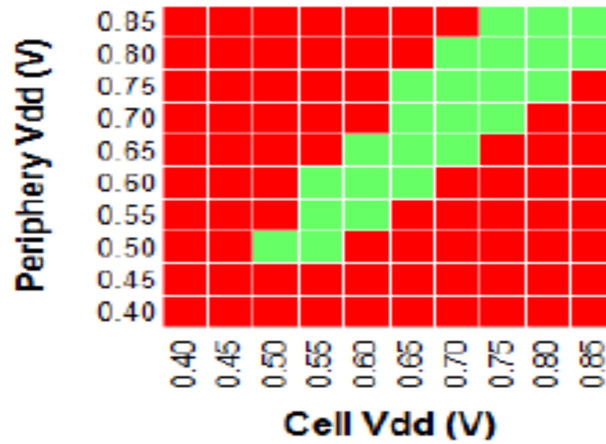


Paper T2.1, Figure 7 – "Si FinFET-based 10nm Technology with Multi V_t Gate Stack for Low Power and High Performance Applications," Cho et al., Samsung Electronics

TSMC will demonstrate a fully functional 32Mb 6-T high density SRAM with smallest reported size of sub-0.03μm^2 using bulk CMOS FinFETs scaled beyond the 10nm node.

This presentation also reports improved transistor performance and electrostatic control through process and CET optimization of scaled FinFETs with competitive performance: DIBL of

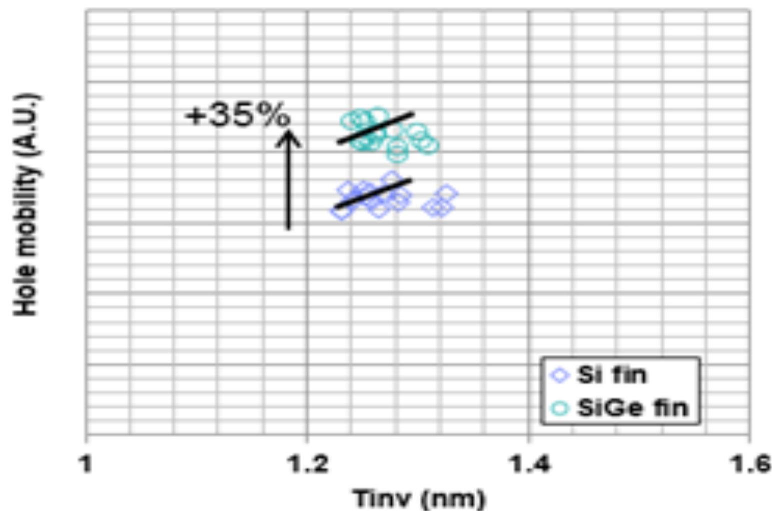
<45mV/V, sub-threshold swing of <65mV/decade, and static noise margin of ~90mV for the high density SRAM operated at 0.45V.



Paper T9.1, Figure 15 - "Demonstration of a Sub-0.03 um^2 High Density 6-T SRAM with Scaled Bulk FinFETs for Mobile SOC Applications Beyond 10nm Node," Wu et al., TSMC

IBM and GLOBALFOUNDRIES developed the fundamental and disruptive enhancement of transistor mobility needed to continue expected power and performance scaling at 10nm and beyond, with the introduction of high mobility SiGe channel (20%Ge) into the PFETs to achieve 35% hole mobility increase, and thus ~17% PFET I_{eff} enhancement.

The presentation will demonstrate for the first time10nm FinFET CMOS technology featuring SiGe channel PFETs with superior NBTi reliability and defect control.



T2.2, Figure 8 – "FINFET Technology Featuring High Mobility SiGe Channel for 10nm and Beyond," Guo, et al., IBM and GLOBALFOUNDRIES

B) Advanced Technology Using New Channel Materials & New Device Structures

TSMC will present a systematic study of the material properties, dimension effects and device characteristics of its In0.53Ga0.47As FinFETs, manufactured on 300mm Si substrates that demonstrate high performance with good uniformity across the wafer. High electron mobility III-V semiconductors are one potential path for continuing Moore's Law to meet the high performance and low power requirements of future logic applications. Creating high quality hetero-epitaxial of III-V material on large scale Si platforms with good HK/III-V interfaces are critical hurdles to overcome for fabricating HP devices capable of replacing Si FF as scaling continues beyond 7nm.

Significantly, the devices fabricated on 300mm Si show similar characteristics in SS and I_{on} when benchmarked with equivalent devices fabricated on lattice-matched InP substrates. The current drive of the III-V FinFETs is I_{on}=44.1uA per fin for a fin-height of 70nm and a fin-width of 25nm. These results are among the highest values reported for In0.53Ga0.47As FinFETs.

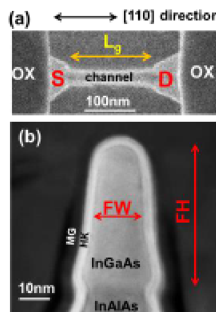


Fig. 2 (a) Top view SEM and (b) cross-sectional TEM images of the InGaAs FinFET.

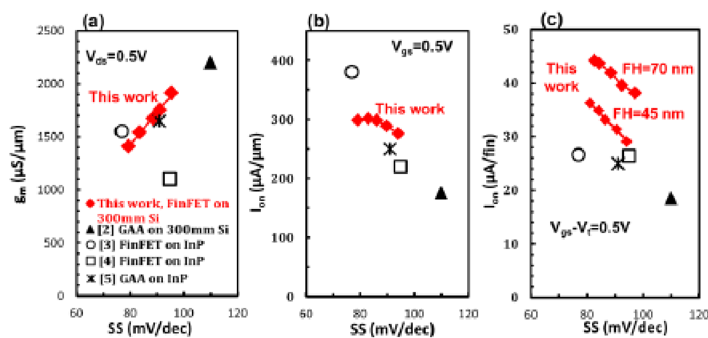


Fig. 14 Benchmarking of g_m (a) and I_{on} (b,c) vs. SS of $In_{0.53}Ga_{0.47}As$ Fin- and nanowire- FET at V_{ds}=0.5V and V_{gs}=0.5V with I_{off}=100nA/um. The g_m and I_{on} data are selected from device FW=20-50 nm.

Paper T2-3, Figures 2 & 14 – "High Performance In0.53Ga0.47As FinFETs Fabricated on 300mm Si Substrate" by M.L. Huang et al., TSMC

Researchers at **IBM** will demonstrate for the first time high Ge content (HGC) SiGe FinFETs in a replacement mode high-k and metal gate (RMG) process flow with an aggressive equivalent oxide thickness (EOT) scaling down to 0.7nm. IBM's first of its kind HGC SiGe pMOS FinFETs exhibits high mobility, record-low RMG long channel SS=66mV/dec and good short channel behavior down to L_g=21nm.

The devices are characterized down to 4nm fin widths with excellent mobility (μ_{eff}=220cm^2/V-s) and reliability at 0.7nm. A 10-year lifetime target is achieved for sub-10nm FinFET widths. This work demonstrates best mobility values compared to state-of-the-art FinFETs, ultra thin body Si or Ge alternatives, as well as to strained SiGe quantum well options, showing that

high performance SiGe FinFETs are feasibile at these aggressive dimensions, with results that outperform all previously reported data.

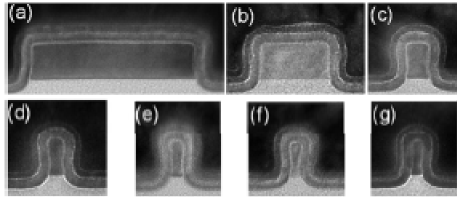


Fig. 2 XTEM of RMG HGC SiGe-OI PMOS FinFETs with W_{FIN} (measured from the center of the fins) = (a) 87nm, (b) 36nm, (c) 10nm, (d) 7nm, (e) ~5nm, (f, g) ~3-3.6nm and H_{FIN}~19.5nm. Fin shown in (g) has a different type of workfunction (WF) setting metal gate. than those in (a-f).

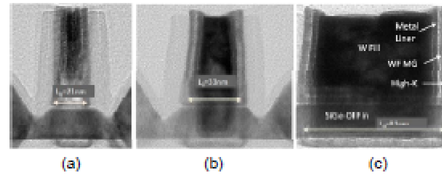


Fig. 3 Cross-section TEM images of RMG HGC SiGe-OI PMOS FinFETs with (a) L_G=21nm, (b) L_G=33nm and (c) L_G=83nm. We have scaled the physical thickness of the WF metal to sub-3nm, which allows us L_G scaling.

Paper T9.3, Figures 2 & 3 – "Replacement High-K/Metal-Gate High-Ge-Content Strained SiGe FinFETs with High Hole Mobility and Excellent SS and Reliability at Aggressive EOT ~7Å and Scaled Dimensions Down to Sub-4nm Fin Widths" by P. Hashemi et al. IBM

A team from **imec** reports on vertically stacked gate-all-around (GAA) n- and p-MOSFETs of 8nm diameter with nanowire stacking and replacement metal gate (RMG) processing, which is relevant for continuing scaling beyond sub-10nm technology.

Stacking nanowire GAA devices is a promising path to maximize current drive per footprint. Fabricated by adapting a RMG FinFET process, these devices represent an evolutionary approach to extend the learning achieved with FinFET manufacturing. The nanowires exhibit excellent short channel characteristics (SS=65mV/dec, DIBL=42mV/V for L_g=24nm) at performance levels comparable to FinFET devices. The parasitic channel below the nanowires is suppressed by a groundplane doping technique prior to nanowire specific processing.

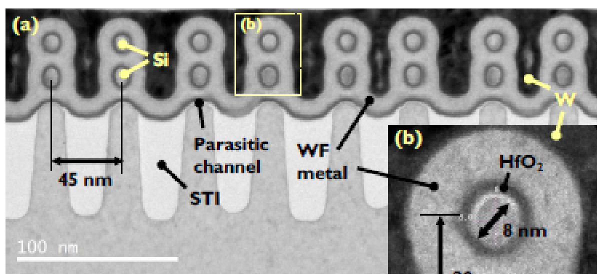


Fig. 2. TEM images of an NMOS GAA Si NWFET (L_G = 70 nm): (a) overview of the Si NW array, and (b) detailed view of two stacked Si NWs. The rounded NW shape, the narrow NW size distribution, and the conformally deposited HK/MG layers are clearly visible.

Paper T15.1, Figure 2 – "Gate-All-Around MOSFETs Based on Vertically Stacked Horizontal Si Nanowires in a Replacement Metal Gate Process on Bulk Si Substrates" by H. Mertens et al., IMEC

Intel's corporate research group shows performance, area, and energy efficiency are improved by novel tunnel FET (TFET) library circuits, redesign of logic at low-V_{DD} and

CMOS/TFET heterogeneous logic. The TFET/CMOS logic with low-overhead level-shifters improves performance 50% while reducing energy 42% for non-critical performance logic. Performance and power are benchmarked by design synthesis using industry test cases, libraries and interconnect.

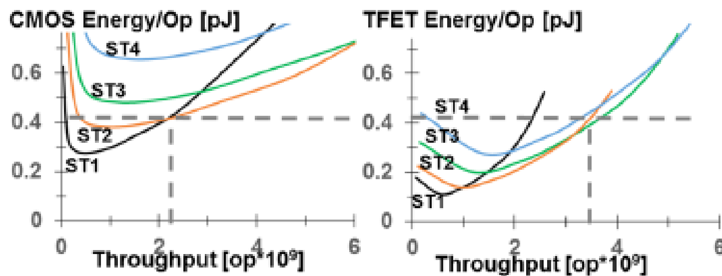


Fig. 9: Interaction between logic-level and low-V_{DD} power-performance. Dashed line indicates an iso-energy/op comparison where TFET exceeds CMOS performance by 45% due to energy-efficient TFET pipelining.

Design	CMOS (0.65 V)	CMOS Multi-V_{DD}	Heterogeneous TFET/CMOS	TFET (0.41 V)	TFET Multi-V_{DD}
Energy/Op 16b MULT	40 fJ	40 fJ (@0.65 V)	40 fJ (@0.65V CMOS)	11 fJ	11 fJ (@0.41 V)
Energy/Op 32b ADD X32	118 fJ	52 fJ (@0.45 V)	30 fJ (@0.32V TFET)	39 fJ	24 fJ (@0.32 V)
Frequency	3.3 Ghz	3.3 Ghz	3.3 Ghz	2.2 Ghz (below spec)	2.2 Ghz (below spec)
Energy/Op Total	158 fJ	92 fJ	70 fJ	50 fJ	35 fJ

Fig. 10: Heterogeneous CMOS/TFET extends logic performance range by 50% and provides 42% energy savings on non-critical performance logic.

Paper T21.1, Figures 9 & 10 – "Enabling High-Performance Heterogeneous TFET/CMOS Logic with Novel Circuits Using TFET Unidirectionality and Low-VDD Operation" by D.H. Morris et al., Intel

C) Advanced Non-Volatile Memory Technology (MRAM & PCM) Introduced in Products

TDK Headway Technologies returns to the VLSI Symposium to present advances in writing speed of their perpendicular spin-transfer torque magnetic memory (pSTT-MRAM), which can be reduced to a pulse width of 750ps without compromising functionality and data retention. The switching of the full 8MB array with 80nm devices can be achieved with 3ns pulses without use of error-correcting code (ECC), with the array level data retention showing a 10-year lifetime at 1ppm at 125ºC.

They demonstrate sub-ns switching of pSTT-MRAM over a large temperature range after optimization of the magnetic tunnel junction (MTJ) stack, with single devices switched reliably using write pulse length down to 750ps while preserving functionality and data retention @125ºC.

This pSTT-MRAM with improved writing speed is a viable candidate for replacement of LCC cache for advanced technology nodes, as well as a possible replacement for non-volatile memory.

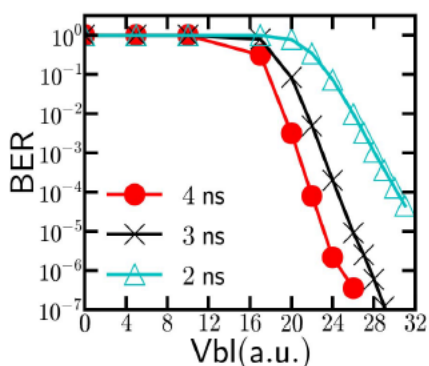


Fig. 12 Write shmoo at short pulses at RT performed on 8MB array. Using 3ns pulses all junctions do write without ECC

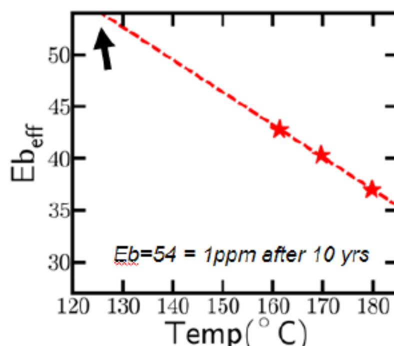
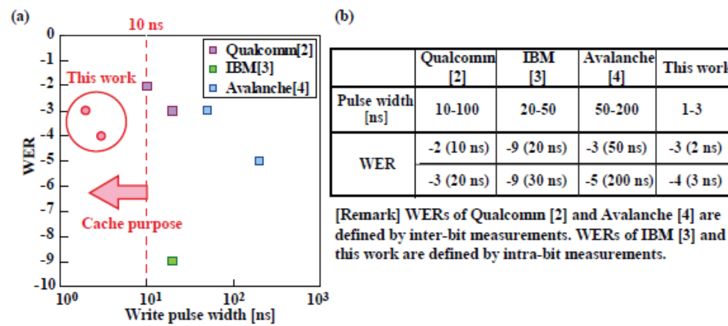


Fig 13 data retention chip level demonstrating 10yr data retention at 125ºC (criteria =1 ppm failure rate after 10 years)

Paper T2.4, Figures 12 & 13 – "Achieving Sub-ns Switching of STT-MRAM for Future Embedded LLC Applications Through Improvement of Nucleation and Propagation Switching Mechanisms" by G. Jan et. al., TDK-Headway Technologies

A novel perpendicular magnetic tunnel junction (MTJ) is demonstrated by **Toshiba** with a high speed cache memory operation around 1ns, low power switching less than sub-100µA and size scalability of write current down to 16nm diameter MTJ. This novel MTJ is suited for embedded NVRAM solutions for sub-20nm high-performance CMOS SoC technology.



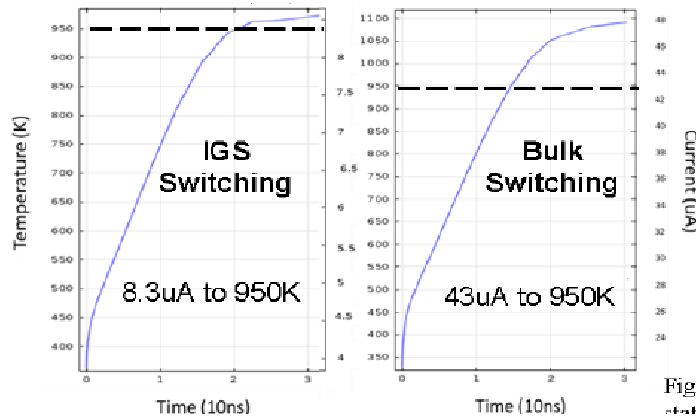
	Qualcomm [2]	IBM [3]	Avalanche [4]	This work
Pulse width [ns]	10-100	20-50	50-200	1-3
WER	-2 (10 ns)	-9 (20 ns)	-3 (50 ns)	-3 (2 ns)
	-3 (20 ns)	-9 (30 ns)	-5 (200 ns)	-4 (3 ns)

[Remark] WERs of Qualcomm [2] and Avalanche [4] are defined by inter-bit measurements. WERs of IBM [3] and this work are defined by intra-bit measurements.

Fig. 14 (a) Comparison of WER between previous work and this study. (b) Table of comparison in device features. High WER down to 2 ns was achieved in our work.

Paper T14.2, Figure 14 – "Sub-3ns Pulse with Sub-100µA Switching of 1x-2xnm Perpendicular MTJ for High-Performance Embedded STT-MRAM Towards Sub-20nm CMOS" by Daisuke Saida et. al., Toshiba Corporation

Macronix and **IBM** investigate methods of reducing programming power in phase change memories (PCM) for new storage class memory (SCM) applications. The researchers demonstrate a new low power phase change memory using inter-granular switching (IGS), a novel 3D network of crystallites with phase change confined to grain intersections. Contrary to conventional phase change memories, for which an entire volume of chalcogenide glass is amorphized or crystallized to achieve high or low resistance, they propose a multi-grained structure where the phase change occurs only in the inter-grain regions. By localizing the phase-change to the inter-grain area, the reset power is substantially reduced to 20µA, as well as the thermal disturbance to the neighboring bits, with set speed and cycling endurance also enhanced.



Paper T12.4, Figure 5 – "A Novel Low Power Phase Change Memory Using Inter-Granular Switching" by H.L. Lung et. al., Macronix International and IBM

D) Advancing Beyond Scaling Using Orthogonal Technologies Such As 3D Integration

CEA Leti and **STMicroelectronics** demonstrate for the first time a full 3D VLSI CMOS-over-CMOS integration, CoolCube™, on 300mm wafers, with the top level CMOS devices fabricated using low temperature (less than 650°C) processes. A functional 3D inverter with either PMOS over NMOS or NMOS over PMOS is demonstrated to achieve compatible performance with state-of-the-art high performance FDSOI devices. Furthermore, the Leti/STM work demonstrates the integration feasibility of CoolCube™ by transferring a high quality Si layer over the 28nm devices with W-M1 and then returning to the front end of the line for processing the top CMOS devices.

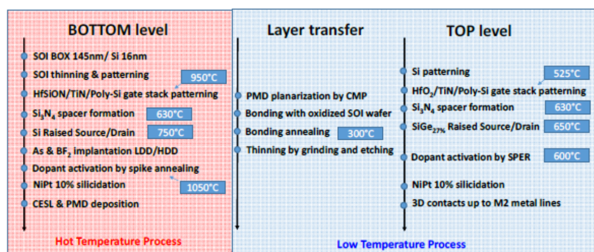


Fig.1: Process flow scheme of 3D CoolCube™ integration: bottom level realization at high temperature, layer transfer and realization of the top level at low thermal budget.

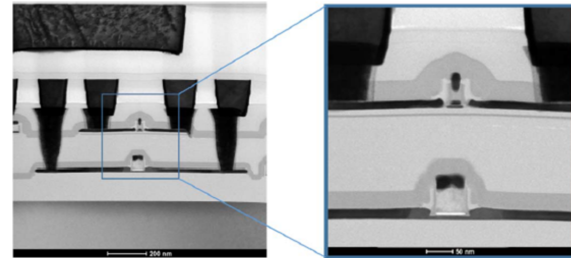
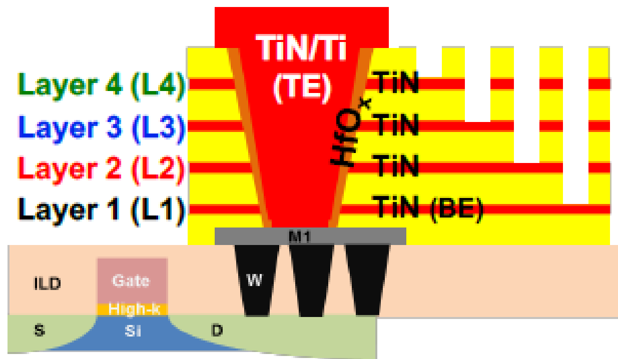


Fig.2: TEM cross-section of the 3D sequential structure up to M2 line. Nanometric top and bottom transistors alignment is observed.

Paper T17.3, Figures 1 & 2 – "First Demonstration of a CMOS-Over-CMOS 3D VLSI CoolCube™ Integration on 300mm Wafers," by L. Brunet et.al., CEA Leti and STMicroelectronics

For the first time, researchers at **Stanford** and **National Nano Device Laboratories** have developed a four-layer HfO_x-based 3D vertical RRAM, the "tallest" one ever reported, integrated with FinFET selector. The four-layer 3D RRAM is a versatile computing unit for (a) brain-inspired computing and (b) in-memory computing. Uniform memory performance across four layers is obtained (±0.8V switching, 10^6 endurance, 10^4s @125°C). The 3D architecture with dense and balanced neuron-synapse connections provides 55% energy delay product (EDP) savings and 74% V_{DD} reduction (enhanced robustness) as compared with conventional 2D architecture.



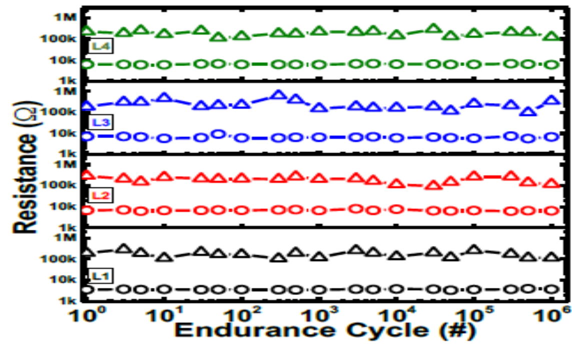


Fig. 6 Measured endurance characteristics. None of four cells show degradation after 10^6 cycles. Besides, consecutive switching is disturb-free on adjacent layers.

Paper T18.2, Figures 1 & 6 – "Four-Layer 3D Vertical RRAM Integrated with FinFET as a Versatile Computing Unit for Brain-Inspired Cognitive Information Processing" by Haitong Li et.al., Stanford University and National Nano Device Laboratories

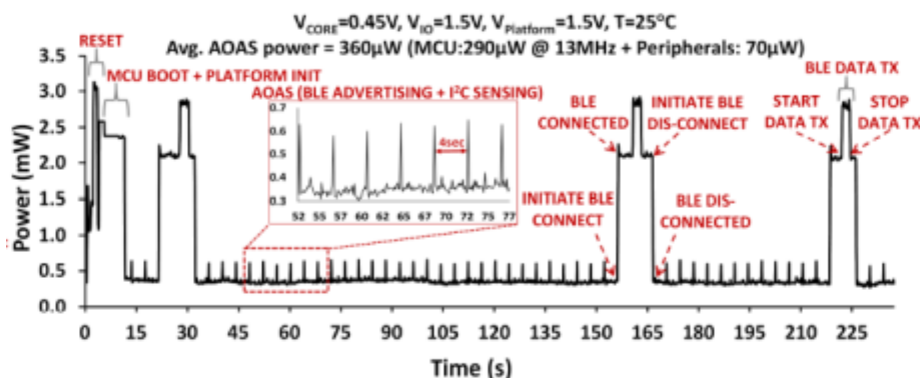
II) Technical Highlights from the Symposium on VLSI Circuits

The 2016 Symposium on VLSI Circuits is part of a premiere international conference that defines the pace, progress and evolution of microelectronics, scheduled from June 14-17, 2016 in Honolulu, Hawaii and held in conjunction with the Symposium on VLSI Technology (June 13-16, 2016). The Symposia's overall theme "Inflections for a Smart Society," reflects the industry's transition point as "smart" system level applications help to transform the industry. Following are some of the highlighted papers that address this theme:

A) Internet of Things

In the future "Smart Society," a proliferation of intelligent devices will be wirelessly interconnected in the Internet of Things. Advances in computation, sensing, and wireless connectivity will enable low-power sensor nodes that can be deployed in applications ranging from ambient intelligence to health monitoring. A focus session "Innovative Systems for a Smart Society," highlights several such systems, with additional IoT-focused papers throughout the Symposium.

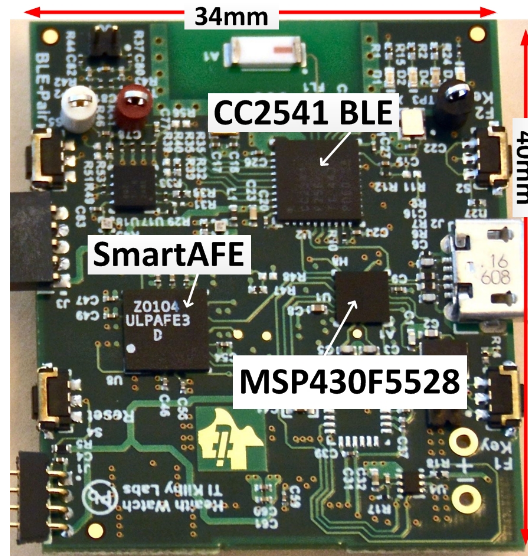
Built around a near-threshold voltage microcontroller, **Intel** demonstrates an energy harvesting sensor node that includes a solar cell, energy harvester, flash memory, and a BLE (Bluetooth Low Energy) radio. Implemented in 14nm tri-gate CMOS, the IA-32 MCU can operate to the peak energy efficiency point of 308mV supply, consuming just 17pJ/cycle. In indoor lighting environments, the sensor node operates continuously in an "always-on-always-sensing" state, with continuous reporting of sensor data to the cloud. ***(Paper C8.1, Figure 12 – "An Energy Harvesting Wireless Sensor Node for IoT Systems Featuring a Near-Threshold Voltage IA-32 Microcontroller in 14nm Tri-Gate CMOS," S. Paul, et al., Intel Corporation)***



Intel will present an energy-harvesting sensor node that can operate continuously in 1000lux indoor lighting scenarios, featuring a 14nm near-threshold voltage IA-32 MCU. The above figure shows the power profile of continuous sensing and periodic wireless reporting of the data.

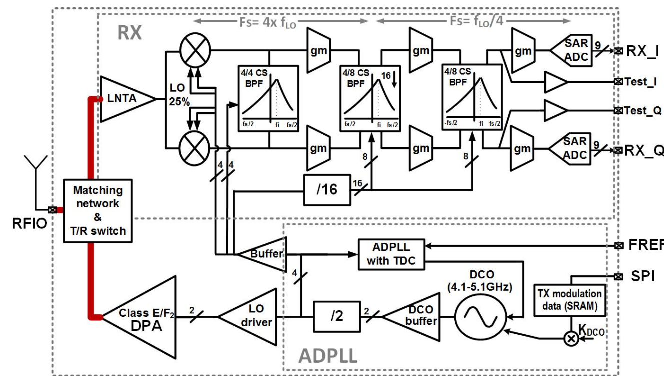
Texas Instruments will demonstrate a multi-modal bio-sensing platform that can synchronously capture electrocardiography (ECG) and photoplethysmography (PPG) data with applications for health, fitness, and mobile patient monitoring. The ultra-low-power frontend can be adapted "on-the-fly" with background cancellation and input-signal-aware data-path adaptation while maintaining >80dB SNR. Paired with a low-power MCU and BLE radio, the full node can operate for three days from a coin cell battery. ***(Paper C8.4, Figure 6 – "Multi-***

modal Smart Bio-sensing SoC Platform with >80dB SNR 35µA PPG RX Chain," A. Sharma, et al., Texas Instruments)



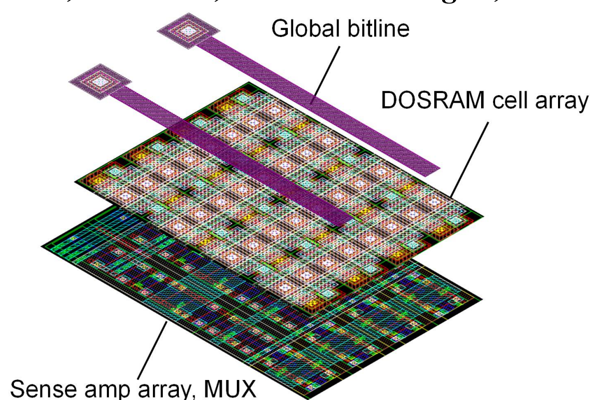
Texas Instruments demonstrates an adaptive analog front-end (AFE) that draws 35uAfor PPG sensing. Shown above is the entire sensor platform that further includes a BLE radio and MSP430 MCU and operates from a coin cell battery.

Bluetooth Low-Energy (BLE) is one of the most prominent technologies for connecting sensor nodes to the cloud, due to its low-power dissipation and presence on many smart phones, enabling their function as a mobile gateway. A group of researchers from **TSMC, Delft University of Technology, Federal University of Rio Grande do Sul**, and **University College Dublin** demonstrate a BLE transceiver that uses a high-rate discrete-time baseband with multi-stage multi-rate charge-sharing bandpass filters to achieve robust out-of-band linearity to reduce interference. The radio also includes a TX/RX switch and all matching components necessary to directly interface with a minimum size BLE radio antenna. The transceiver consumes 2.75mW and 3.6mW in RX and TX modes, respectively. ***(C7.1, Figure 1 – "A Bluetooth Low-Energy (BLE) Transceiver with TX/RX Switchable On-Chip Matching Network, 2.75mW High-IF Discrete-Time Receiver, and 3.6mW All-Digital Transmitter," F.-W. Kuo, et al., TSMC, Federal University of Rio Grande do Sul, Delft University of Technology, University College Dublin)***



The above figure shows a BLE transceiver supporting a direct single-pin antenna interface by embedding a matching network and switch between its discrete-time BB RX chain and ADPLL-based TX.

In addition to IoT systems built in CMOS, new technologies can provide additional capabilities to achieve ultra-low power dissipation. The **Semiconductor Energy Laboratory Co.**, **UMC, ARM, Nokia Techologies**, and **The University of Tokyo** will present c-axis aligned crystalline indium-gallium-zinc oxide (CAAC-IGZO) FETs within the memory and flip-flops of an ARM Cortex M0 processor. These CAAC-IGZO FETs provide extremely low off-state current and are stacked on top of the CMOS circuits, creating no area overhead. The memory and M0 core achieve 3 and 6nW of standby power, respectively. The active memory power is also reduced to 11.7µW/MHz by minimizing the bitline to the length of the sense amplifier. This reduced standby power dissipation allows efficient computation over wide ranges of duty cycles as seen in many IoT applications. ***(C12.2, Figure 5 - "Embedded Memory and ARM Cortex-M0 Core Using 60nm C-Axis Aligned Crystalline Indium–Gallium–Zinc Oxide FET Integrated with 65nm Si CMOS," T. Onuki, et al., Semiconductor Energy Laboratory Co., United Microelectronics Corporation, ARM Ltd., Nokia Technologies, The University of Tokyo)***

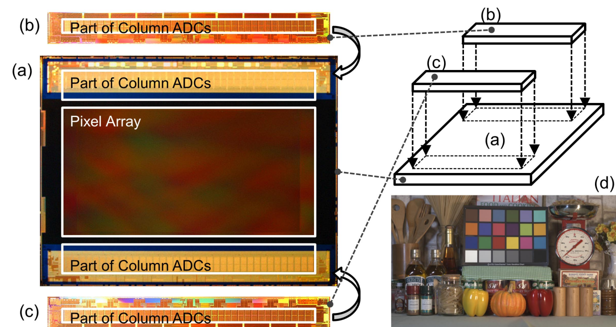


The above figure shows the layout of the CAAC-IGZO DRAM-type memory array stacked on top of the CMOS sense amplifiers.

B) Image Sensors

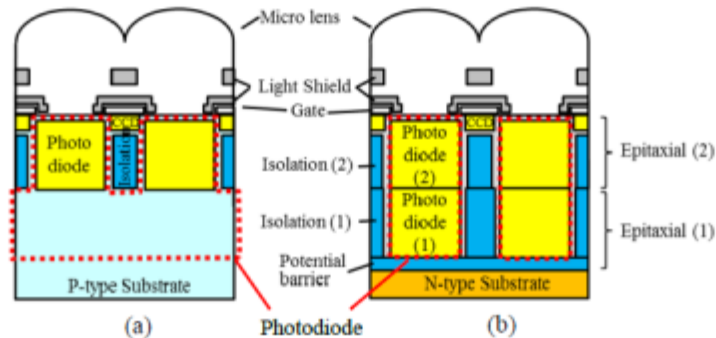
Imagers represent the sensing interface that most directly correlates to how humans sense the world. Multiple "More-than-Moore" techniques, including novel photodiode structures, 3-D integration, and diffraction gratings that achieve superior sensitivity and speed are demonstrated in the highlighted papers below.

For video cameras that do not support mechanical shutters, a global electrical shutter is essential to eliminate the motion blur seen with rolling shutters. **Sony** demonstrates a CMOS image sensor for next generation immersive user viewing experiences with 4K high definition video and up to 480fps (frames per second) for slow-motion instant replays. Low dark random noise of 140µV_{rms} is achieved using gain-adaptive column ADCs stacked on top of the image sensor, with the best dynamic range among high-speed image sensors with large optical format. This work shows the potential for CMOS to displace CCD-based imagers in this application. ***(C21.1, Figure 4 – "An 8.3M-pixel 480fps Global-Shutter CMOS Image Sensor with Gain-Adaptive Column ADCs and 2-on-1 Stacked Device Structure," Y. Oike et al., Sony)***



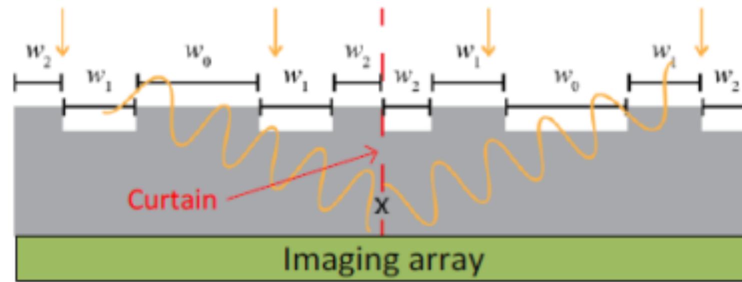
This figure shows a Sony image sensor with global shutter, 8.3M-pixel, and 480 frames per second. The gain adaptive column ADCs are used to extend the dynamic range and are implemented in a stacked configuration along the periphery of the array.

Near-IR light is widely used in surveillance, time-of-flight, and automotive applications. **TowerJazz Panasonic** and **Panasonic Semiconductor Solutions** have implemented a 10µm deep photodiode that improves the quantum efficiency at 850nm by almost 2x compared to a traditional depth photodiode. Through a two-step epitaxial process on an n-type substrate, each stacked photodiode is completely separated from neighboring pixels, maintaining a 40% modulation transfer function and no degradation in dark current. ***(T22.1 - "Novel Pixel Structure with Stacked Deep Photodiode to Achieve High NIR Sensitivity and High MTF," H. Takahashi, et al., TowerJazz Panasonic, Panasonic)***



The above figure shows a comparison of (a) conventional photodiode with limited depth and (b) the new stacked, fully isolated deep photodiode developed by TowerJazz.

An invited paper by **Rambus** presents an overview of lensless smart sensors that rely on phase-modulated diffraction gratings above a conventional imaging array. Compared to a lens, this "More-than-Moore" diffraction grating can be designed for wide wavelength bands and has a lower profile for thinner sensors. Point range finding, eye tracking, and occupancy detection applications are discussed. Because the desired information can be directly extracted from the raw image sensor data without full image reconstruction, privacy can be preserved. ***(C8.2, Figure 2 – "Lensless Smart Sensors: Optical and Thermal Sensing for the Internet of Things," P. Gill and T. Vogelsang, Rambus Inc.)***

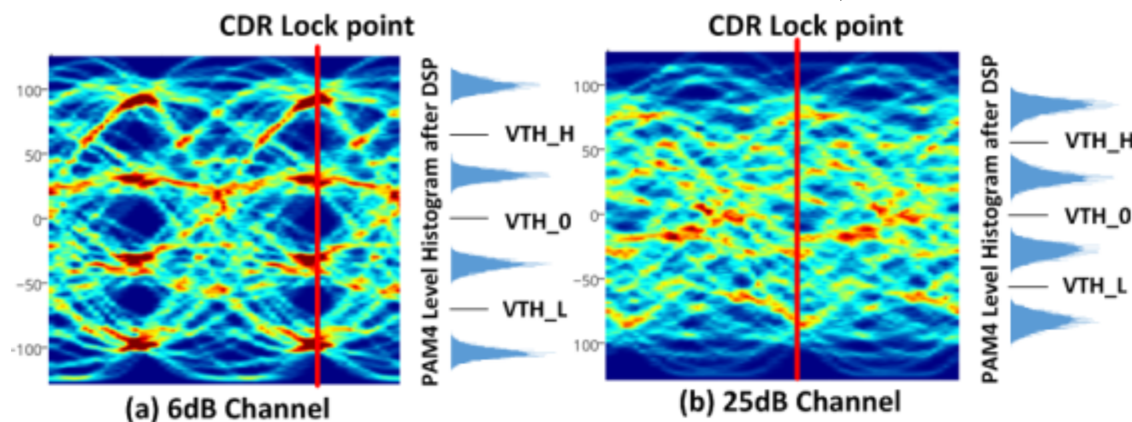


The above figure shows an example phase-modulated diffraction grating for Lensless Smart Sensors.

C) Innovations for the Cloud

The computational backbone of the future smart society resides in "compute farms" within the cloud. New techniques are required to transport and process the immense amount of data coming from the Internet of Things.

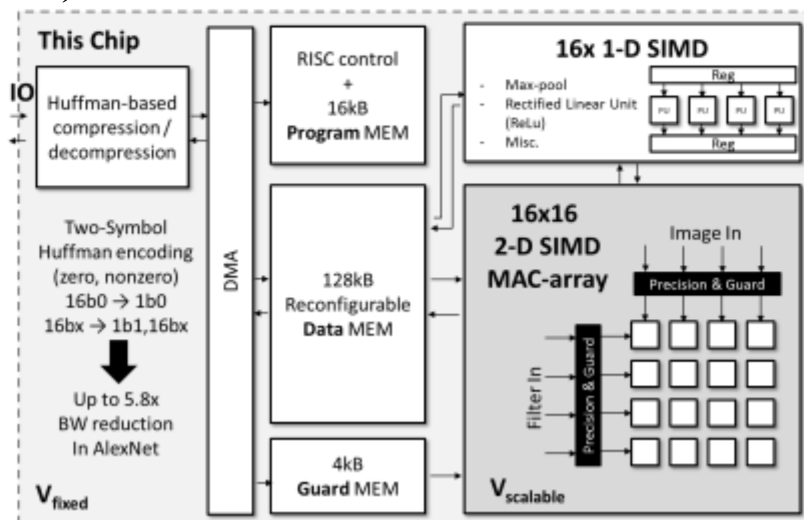
Xilinx will present a 56Gb/s wireline transceiver with 4-level pulse amplitude modulation (PAM4) signaling to support communication over the limited electrical bandwidth of legacy backplanes, thus extending the life of compute farms. The transmitter uses auxiliary current injection to maintain PAM4 amplitude linearity. The DSP-based receiver is based on a 28-GS/s 32-way time-interleaved SAR ADC, and 56Gb/s operation is achieved on channel with 25dB loss at 14GHz. ***(C5.4, Figure 8 - "A 56Gb/s PAM4 Wireline Transceiver using a 32-way Time-Interleaved SAR ADC in 16nm FinFET," Y. Frans, et al.)***



This figure shows the eye diagrams processed at the ADC in the 56Gb/s PAM4 transceiver. The post-DSP levels show support 1e-8 BER with the 25dB loss channel on the right.

Convolutional neural networks (CNNs) have emerged as state-of-the-art classification algorithms for applications ranging from speech-recognition to visual-detection; however, they do not efficiently map to conventional microprocessors. Researchers from **KU Leuven** demonstrate a low-power process for CNNs that achieves 102GOPS and between 0.3-2.6TOPS/W. The processor exploits sparsity of convolutions to reduce memory, and provides precision-scalability that works with supply-scaling to achieve an overall improvement in energy efficiency of 3.9x compared to existing state-of-the-art. ***(C17.1, Figure 2 – "A 0.3-2.6 TOPS/W***

Precision-Scalable Processor for Real-Time Large-Scale ConvNets," B. Moons and M. Verhelst, KU Leuven.)

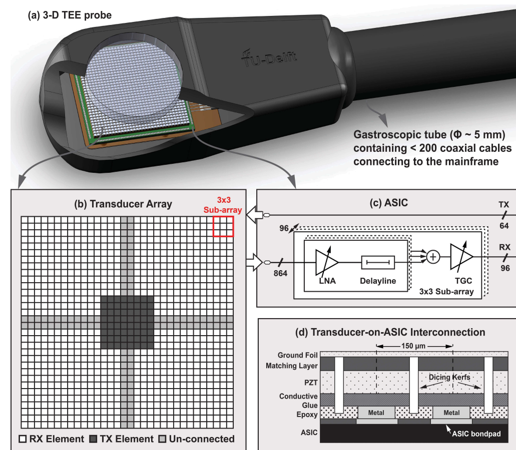


Above shows the top-level architecture of the CNN-processor, including the partition between fixed and scalable power domains.

D) Healthcare and Bio-sensing

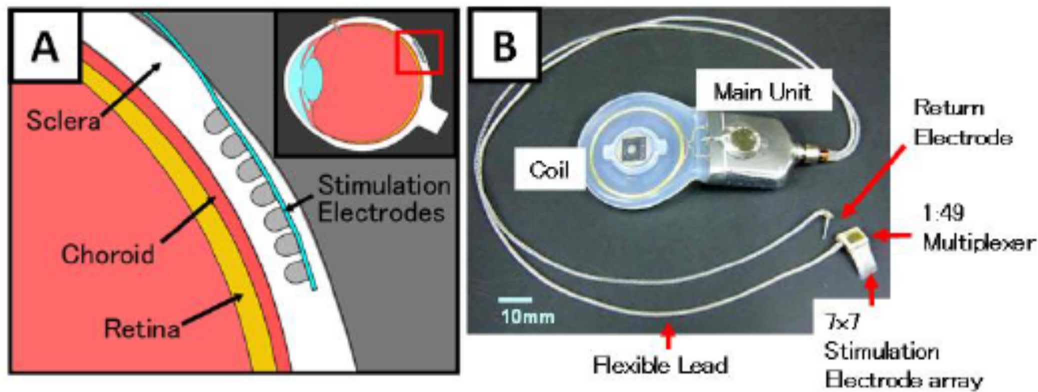
While novel sensor platforms show how the IoT intersects with continuous health monitoring, semiconductor technology can further improve existing systems, or create new diagnostic and prosthetic capabilities. These typically use "More than Moore" techniques of integration with non-CMOS sensors, actuators, as shown in the examples highlighted below.

Delft University of Technology, Erasmus Medical Center, and **Oldelft Ultrasound** present a front-end ASIC for a 3-D transesophageal echocardiography. This ASIC, interfaced to a 1024-element ultrasonic transducer, images the heart from the esophagus. By moving 3x3 beamformers into the front-end ASIC, the number of cables through the gastroscopic tube is reduced by more than 6x, critical for allowing access into the esophagus. Mismatch scrambling eliminates interfering tones from the beamformers' delay lines. ***(C4.4, Figure 1 - "A Front-end ASIC with Receive Sub-Array Beamforming Integrated with a 32 × 32 PZT Matrix Transducer for 3-D Transesophageal Echocardiography," C. Chen, et al., Delft University of Technology, Erasmus MC, and Oldelft Ultrasound)***



This figure shows the miniature transesophageal echocardiography probe and tube, along with the transducer array configuration, ASIC design, and interconnection between the two.

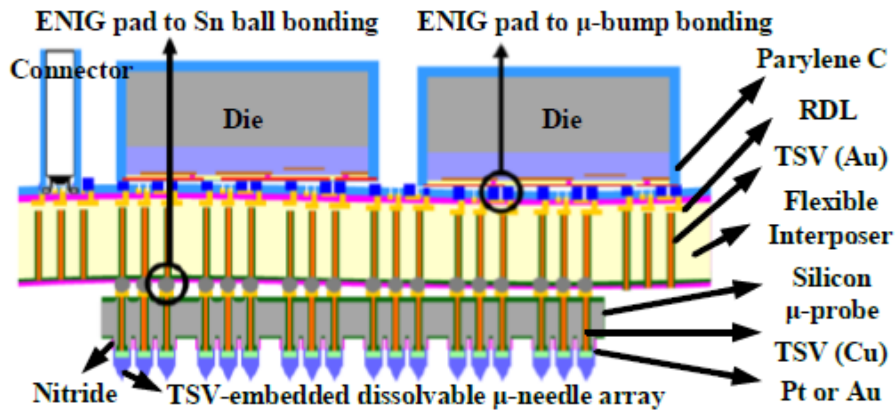
In an invited paper, **NIDEK** and **Nara Institute of Science & Technology** describe a retinal prosthesis for restoring limited visual information to patients with acquired blindness. Suprachoroidal transretinal stimulation (STS) is used in human clinical trials and is deemed safe and effective. As electrode counts increase in next generation systems, the architecture for implanted systems must evolve. The multiplexer will move from the main unit behind the ear into the electrode array within the eye. Safety concerns are addressed, including AC power and data transfer, charge balancing, and prevention of current leakage due to broken electrodes. The 49-channel array is demonstrated *in vitro* and *in vivo*. ***(C8.3, Figure 1 - "Features of Retinal Prosthesis Using Suprachoroidal Transretinal Stimulation from an Electrical Circuit Perspective," Y. Terasawa, et al., NIDEK Co Ltd., Nara Institute of Science & Technology)***



The suprachoroidal transretinal stimulation system includes stimulation electrodes embedded in the sclera, connected through a flexible lead to the main unit implanted behind the ear, wirelessly coupled to an external coil for data and power.

While still in their infancy, neural implants have the potential to lead to treatments for Parkinson's disease and other movement disorders. To understand local brain connectivity, high-density electrode arrays are needed. **National Chiao Tung University** and **China Medical University** show a neural sensing microsystem that employs vertical integration with dissolvable

μ-needles connected through a flexible interposer to ultra-low power recording circuits. Au-TSVs replace copper in the interposer for biocompatibility. The vertical integration path not only minimizes dimension, reducing surgical area and promoting success rate, but also reduces loss between the needles and the sensing circuit to improve sensitivity. A 256-channel array at 288μm electrode pitch is demonstrated. ***(T20.4, Figure 2 - "Integration of Neural Sensing Microsystem with TSV-embedded Dissolvable μ-Needles Array, Biocompatible Flexible Interposer, and Neural Recording Circuits," Y.-C. Huang, et al., National Chiao Tung University and China Medical University)***



This figure shows the vertical integration of the dissolvable μ-needles, flexible interposer, and low-power neural recording dies.

###