2017 Symposia on VLSI Technology and Circuits June 5th (Monday)

2017 Symposium on VLSI Techonlogy / Circuits June 9th (Friday)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I	Time	Suzaku I, II, III
7:30-18:00	I		Registration (Technology a	nd Circuits)	·			
8:30-10:10		 2017 Symposium on VLSI Circuits Short Course 2 Integrated Circuits for Smart Connected Cars and Automated Driving 8:30 Brief Outline, Short Course Chair 8:35 An Overview of Automotive Electronics, C. Lang, Bosch USA 	 2017 Symposium on VLSI Circuits Short Course 1 Machine Learning for Circuit Designers 8:30 Brief Outline, Short Course Chair 8:35 Machine Learning Basics and Its Applications to Internet-of-Things, H. Maruyama, Preferred Networks 	2017 Symposium on VL Technology Enablers for 5i 8:30 Introduction 8:35 CMOS Device Technology Enal P. Hashemi and T. B. Hook, IBM	SI Technology Short Course nm and Next Wave of Integration blers and Challenges for 5nm Node, Research		9:00-12:00	International Forum on Singularity: Exponential X (Friday Forum) 09:00 Welcome to Exponential X, K. Yano, Hitachi Session 1. Exponential Technology 09:15 Exponential Neuromorphic Systems for Singularity, V. De, Intel
	Demo Setup	9:25 Intra-Vehicle Wireline Networks, A. Klaus, Marvell Semiconductor 10:15 Break	 9:25 Machine-Learning-Enabled Design Space for Energy-Efficient Mixed-Signal Inference Systems, N. Verma, Princeton Univ. 10:15 Break 	 9:25 Heterogeneous Integration of C from More Moore to Beyond (M. Takenaka, The Univ. of Tokyo 10:15 Break 	ie, III-V, and 2D on Si CMOS –,			 09:45 Exponential Computing for Singularity, M. Saito, PEZY 10:15 Exponential Connectivity for Singularity, A. Amerasekera, UCB/BWRC
10:30-12:10		 10:35 Image Sensors for Automotive Applications, S. Kawahito, Shizuoka Univ. 11:25 LIDAR System Design for Automotive Applications, E. Bartolome, Texas Instruments 	 10:35 Designing Efficient Deep Learning Accelerators: Challenges and Opportunities, J. Emer, Massachusetts Institute of Technology / nVidia 11:25 Advanced Techniques for High-Speed Deep Learning on Large-Scale Neural Network in the Cloud, Y. Tomita, Fujitsu Laboratories Ltd. 	 10:35 Design & Technology Co-Optin P. Penzes, Qualcomm Technolog 11:25 The Duality of Interconnect Sca Increasingly Complex, Increasi R. Fox, GLOBALFOUNDRIES 	nization for High Performance SoC, jies, Inc. aling in Sub-10nm Technology Nodes: ngly Important,	8:30-17:40 2017 Silicon Nanoelectronics Workshop (Day 2)	12:00-13:30	 10:45 Exponential Commerce for Singularity, T. Kitagawa, Rakuten 11:15 Panel "Where will the Next Exponential Technology Arise?" 12:00 Lunch Time Session 2. Exponential Humans
12:10-13:30		12:15 Lunch	12:15 Lunch	12:15 Lunch				 13:30 Exponential Intelligence for Singularity, K. Ataka, Yahoo
13:30-16:00		 13:30 Automotive Sensors and Interfaces, B. Clark, Analog Devices, Inc. 14:20 Key Technologies That Support EV Motor Control, S. Otani, Renesas Electronics Corp. 15:10 Break 	 13:30 Deep Learning for Mobile and Embedded Devices, M. Aleksic, Qualcomm Inc. 14:20 Vision-Centric Devices at the Network Edge Using Deep-Networks and Computer Vision, D. Moloney, Intel Corp. / Movidius 15:10 Break 	 13:30 Heterogeneous 3D/2.5D Integra M. Koyanagi, Tohoku Univ. 14:20 Device Challenges for Scaled A FL. Hsueh, YC. Peng, JJ. Ho B. Yang, V. Chou, A. Kundu, CT HH. Hsieh, CH. Chang, YW. 15:10 Break 	tion toward IoT and Al Era, malog-RF, mg, WC. Chen, S. Yang, H. Liu, Lu, MC. Chuang, CH. Chen, Chen, LC.Cho, J. Fu and J. Tsai, TSMC		13:30-16:30	 14:00 Exponential Healthcare for Singularity, Y. Ishikawa 14:30 Exponential Mind for Singularity, J. Tani, KAIST 15:00 Exponential Robotics for Singularity, K. Kanaoka, Ritsumeikan Univ.
16:00-17:10		15:30 Autonomous Vehicles Platform: Processor/Software Architecture, Machine Learning and Security, J. Weast, Intel Corp. Demo Setu	15:30 Mobile/Embedded DNN and Al SoCs, HJ. Yoo, KAIST	 15:30 Embedded Memory Design - Memories Differentiate Microor T. Jew, NXP Semiconductors 16:20 On Die Processing in Memory - 	contoller Solutions –, - PIM on DRAM –, F. Devaux, uPmem			15:30 Break 15:45 Panel "How will Human Beings Change in the Future?"
17:30-22:10		17:30-19: Demo Session & F	i0 Reception			19:00-22:10?? 2017 Spinters in		
						Spintronics Workshop on LSI		

2017 Symposia on VLSI Technology and Circuits June 6th (Tuesday)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III Shunju II	Shunju I			
7:00-17:00		·	Registration (Technology and Circuits)					
				T1 "Welcome and Plenary Session"				
				T1-1 8:00-8:45 Welcome and Opening Remarks				
8:00-10:05				SoftBank 5G and It's Surrounding Situations until 2020				
	•			NXP Semiconductors Privacy and Security: Key Requirements for Sustainable IoT Growth				
				C1-1 10:30-10:50 Welcome and Opening Remarks C1-2 10:50-11:40 (Plenary)				
10:30-12:30				Panasonic Innovative Solutions toward Future Society whth AI, Robotics, and IoT C1-3 11:40-12:30 (Plenary)				
				Waymo Inside Waymo's Self-Driving Car: My Favorite Transistors				
12:30-14:00	C2: Machine / Deep Learning	C2: Dalta Sigma Madulatora	C4. Diamodical Circuita and Systems	T2: (FC) Nervalstile & Embadded Memory	T2- III V			
	C2: Machine / Deep Learning C2-1 14:00-14:25	C3-1 14:00-14:25	C4: Biomedical Circuits and Systems	T2-1 14:00-14:25 (Invited)	T3-1 14:00-14:25			
	BRein Memory: A 13-Layer 4.2 K Neuron/0.8 M Hokkaido Synapse Binary/Ternary Reconfigurable In- Univ. Memory Deep Neural Network Accelerator in 65 nm CMOS	KAIST A 4.2mW 10MHz BW 74.4dB SNDR Fourth-Order CT DSM with Second-Order Digital Noise Coupling Utilizing an 8b SAR ADC	National A Fully Integrated Closed-Loop Neuromodulation SoC with Wireless Power and Bi-Directional Data Telemetry for Real-Time Human Epileptic Seizure Tung Univ. Control	KU Leuven and imec Memory Technology for the Terabit Era: from 2D to 3D	Record Performance for Junctionless Lund Univ. Transistors in InGaAs MOSFETs			
	C2-2 14:25-14:50	C3-2 14:25-14:50	C4-2 14:25-14:50	T2-2 14:25-14:50 (Invited)	T3-2 14:25-14:50			
14:00-15:40	Tsinghua Univ. A 1.06-To-5.09 TOPS/W Reconfigurable Hybrid-Neural-Network Processor for Deep Learning Applications	The Univ. A 0.028/mm 19.56/3/86p 2 - Order VCO-based of Texas at Austin Integrator and Capacitive Feedback in 40nm CMOS	National Chiao Tung Univ. A Bone-Guided Cochlear Implant CMOS Microsystem Preserving Acoustic Hearing	TSMC Embedded Memories for Mobile, IoT, Automotive and High Performance Computing	Vertical Heterojunction InAs/InGaAs Lund Univ. Nanowire MOSFETs on Si with I _{on} = 330 μ A/µm at I _{off} = 100 nA/µm and V _D = 0.5V			
	Princeton A Heterogeneous Microprocessor for Energy-Scalable Sensor Inference Using Genetic Programming	C3-3 14:30-15:15 A 5GS/s 156MHz BW 70dB DR Continuous- Univ. of Time Sigma-Delta Modulator with Time- Michigan Interleaved Reference Data-Weighted Averaging	Cortera Neurotech nologies Recording and Stimulation with Rapid Artifact Recovery	NEC A Low-Power Cu Atom Switch Programmable Logic Fabricated in a 40nm-Node CMOS Technology	13-3 14-30-15, 15 15 imec First Demonstration of ~3500 cm²/V-s Electron Mobility and Sufficient BTI Reliability (Max V _{αv} Up to 0.6V) In _{0.5} Ga _{0.47} As nFET Using an IL/LaSIO/Hf0 ₂ Gate Stack			
	C2-4 15:15-15:40 A 3.43TOPS/W 48.9pJ/Pixel 50.1nJ/Classification 512 Analog Neuron Sparse Coding Neural Network Michigan with On-Chip Learning and Classification in 40nm CMOS	C3-4 15:15-15:40 A 55µW 93.1dB-DR 20kHz-BW Single-Bit CT Δ Yonsei Σ Modulator with Negative R-Assisted Univ. Integrator Achieving 178.7dB FoM in 65nm CMOS CMOS	C4-4 15:15-15:40 imec Intraneural Active Probe for Bidirectional Peripheral Nerve Interface	T2-4 15:15-15:40 Scray Semiconductor A Cross Point Cu-ReRAM with a Novel OTS Selector for Storage Class Memory Applications Solutions	T3-4 15:15-15:40 IBM T. J. High Performance and Low Leakage Watson Current InGaAs-on-Silicon FinFETs with 20 nm Gate Length			
	C5: Application Specific I/Os	C6: (CFS) Ultra-Low Power Wireless Transceivers for IoT Systems	C7: Sensor Readout Circuits	T4: (FS) 1D and 2D Atomic Thin Materials and Devices	T5: Hetero Integration			
	C5-1 16:00-16:25 IBM A 5Gb/s 7.1fJ/b/mm 8× Multi-Drop On- Chip 10mm Data Link in 14nm FinFET Research CMOS 2014 A ST/4	C6-1 16:00-16:25 (Invited) Texas Reaching 10-Years of Battery Life for Instruments Industrial IoT Wireless Sensor Networks	C7-1 16:00-16:25 Delft Univ. A Compact Sensor Readout Circuit with of Combined Temperature, Capacitance and Technolow Vetters Conscience Functionality	T4-1 16:00-16:25 (Invited) Duke Univ. Scaling, Stacking, and Printing: How 1D and 2D Nanomaterials still Hold Promise for a New Era of Electronics	T5-1 16:00-16:25 Wafer Level Integration of an Advanced TSMC Logic-Memory System Through 2 nd			
	C5-2 16:25-16:50	C6-2 16:25-16:50	C7-2 16:25-16:50	T4-2 16:25-16:50 (Invited)	Generation CoWoS ⁻ Lechnology			
	Univ. of Minnesota A 10Gb/s 10mm On-Chip Serial Link in 65nm CMOS Featuring a Half-Rate Time- Based Decision Feedback Equalizer	Univ. of A 1.7nW PLL-Assisted Current Injected Michigan 32KHz Crystal Oscillator for IoT	Delft Univ. of Technology Digital Converter with 1.85 nm Resolution	Fujitsu Laboratories One and Two Dimensional Nanocarbon Materials for Innovative Functional Devices	National Enabling Low Power and High Speed Univ. of OEICs: First Monolithic Integration of Singapore InGaAs n-FETs and Lasers on Si Substrate			
16:00-18:05	C5-3 16:50-17:15 An FFE TX with 3.8x Eye Improvement by POSTECH Automatic Impedance Adaptation for Universal Compatibility with Arbitrary Channel and RX Impedances	C6-3 16:50-17:15 A 2.4GHz, -102dBm-Sensitivity, 25kb/s, KAIST 0.466mW Interference Resistant BFSK Multi-Channel Sliding-IF ULP Receiver	C7-3 16:50-17:15 Delft Univ. A CMOS Temperature Sensor with a 49fJ- of Technology K ² Resolution FoM	T4-3 16:50-17:15 Purdue Experimental Demonstration of Electrically-Tunable Bandgap on 2D Black Phosphorus by Quantum Confined Univ. Stark Effect	T5-3 16:50-17:15 Enhancement-Mode N-Channel TFT and Osaka Univ Room-Temperature Near-Infrared Emission Osaka Univ Based on n'/p Junction in Single-Crystalline GeSn on Transparent Substrate Substrate			
	Univ. of A Distance-Immune Low-Power 4-Mbps California, Inductively-Coupled Bidirectional Data Link	C6-4 17:15-17:40 A 16 nm FinFET 0.4 V Inductor-Less Cellular Receiver Front-End with 10 mW Ultra-Low Power and 0.31 mm ² Ultra-Small Area for 5G System in Sub-6 GHz Band	Cr-4 17:15-17:40 National A 0.06mm ² ± 50mV Range -82dB THD Taiwan Chopper VCO-Based Sensor Readout Univ. Circuit in 40nm CMOS	14-4 17:15-17:40 The Univ. Statistical Analyses of Random Telegraph Noise Amplitude in Ultra-Narrow (Deep Sub-10nm) Silicon Nanowire of Tokyo Transistors Transistors	15-4 17:15-17:40 National High V _{th} Enhancement Mode GaN Power Chiao Devices with High I _{D.max} Using Hybrid Tung Univ. Ferroelectric Charge Trap Gate Stack			
	C5-5 17:40-18:05 A 16.6-pJ/b 150-Mb/s Body Channel POSTECH Communication Transceiver with Decision Feedback Equalization Improving >200% Area Efficiency	C6-5 17:40-18:05 (Invited) A Multi-Mode WPAN (Bluetooth, BLE, Broadcom IEEE 802.15.4) SoC for Low-Power and IoT Applications						
18:15-19:30			IEEE SSCS Young Professional					
19:30-20:00	19:30 Symposium o 30th Anniversi	l -20:00 n VLSI Circuits ary Celebration	wentoring Event					
20:00-21:30			20:00-21:30 Circuits Evening Panel Discussion The Most Important Circuits of 2037	20:00-21:30 Joint Evening Panel Discussion How will We Survive the Post-Scaling Era?	20:00-21:30 Technology Evening Panel Discussion Transistor Future; How Does It Evolve after FinFET Era?			

2017 Symposia on VLSI Technology and Circuits June 7th (Wednesday)

Time	Suzaku III		Suzaku II		Suzaku I		Shunju III	Shunju II		Shunju I
7:30-17:00				Registration (Te			gy and Circuits)			
			C8: Pipelined ADCs	C9: S	ensors for Biomedical Applications		T6: Highlight			
		C8-1	8:30-8:55	C9-1	8:30-8:55	T6-1	8:30-8:55			
		imec	A 16nm 69dB SNDR 300MSps ADC with	Arizona	A 1.06 µW Smart ECG Processor in 65 nm	Samsung	Highly Manufacturable 7pm EinEET Technol	pay Featuring FLIV Lithography for Low Power and High Performan	nce Applicat	ions
		imec	Capacitive Reference Stabilization	State Univ	and Personal Cardiac Monitoring	Electronics		by realuring EOV Elitiography for Eow Power and High Performan	ice Applica	lons
		C8-2	8:55-9:20	C9-2	8:55-9:20	T6-2	8:55-9:20			
		KAIOT	A 9.1 ENOB 21.7fJ/conversion-step 10b	Stanford	A High-Precision 36 mm ³ Programmable	Qualcomm	10am Llink Defermence Makile CoC Design	and Taphaolagy Co. Developed for Defermence. Developed Area	Caslina	
8:30-10:10		KAIST	with a Current-Mode Fine ADC in 28nm CMOS	Univ.	Implantable Pressure Sensor with Fully Ultrasonic Power-Up and Data Link	Technologies	Tohim High Performance Mobile Soc Design	and Technology Co-Developed for Performance, Power, and Area	Scaling	
		C8-3	9:20-9:45	C9-3	9:20-9:45	T6-3	9:20-9:45			
		Vrije	A Single-Channel, 600Msps, 12bit,	Univ. of	Chip-Scale Fluorescence Imager for In	National				
		Universitei t Brussel	Ringamp-Based Pipelined ADC in 28nm	California, Berkelev	Vivo Microscopic Cancer Detection	Chiao Tung Univ	First Demonstration of Flash RRAM on Pure	CMOS Logic 14nm FINFET Platform Featuring Excellent Immunity	to Sneak-H	ath and MLC Capability
	C8-4 9:45-10:1		9:45-10:10	C9-4 9:45-10:10		T6-4	9:45-10:10			
		Univ. of	A Calibration-Free 2.3 mW 73.2 dB SNDR 15b	California	A 4uW, ADPLI -Based Implantable	IBM				
		Michigan	100 MS/s Four-Stage Fully Differential Ring Amplifier Based SAR-Assisted Pipeline ADC	Institute of Technology	Amperometric Biosensor in 65nm CMOS	Research	First Demonstration of 3D SRAM Through 3L	Monolithic Integration of InGaAs n-FinFETs on FDSOI Si CMOS	with Inter-La	ayer Contacts
	JFS1: Emerging Reliability Solutions		C10: Frequency Generation		C11: Analog Techniques		T7: Mem	ory 1 PCM ReRAM		T8: Sensing
	JFS1-1 10:30-10:55	C10-1	10:30-10:55	C11-1	10:30-10:55	T7-1	10:30-10:55		T8-1	10:30-10:55
	An Adaptive Clocking Control Circuit with	Tokyo	A Pulse-Tail-Feedback VCO Achieving		A Capacitively-Degenerated 100dB Linear	Univ. of			National	Towards A Fully Integrated, Wirelessly Powered, and
	Laboratories 7.5% Frequency Gain for SPARC Processors	ency Gain for SPARC Institute of FoM of 195dBc/Hz with Flicker Noise Technology Corport of 700Hz		20-150MS/s Dynamic Amplifier		Tsukuba				Ordinarily Equipped On-Lens System for Successive Dry Eye Syndrome Diagnosis
	JFS1-2 10:55-11:20	C10-2 10:55-11:20 C11-2 10:55-11:20 T7-2 10:55-11:20			T8-2 10:55-11:20					
	Statistical Characterization of Radiation-Induced Pulse	Renesas	A 3.2ppm/°C Second-Order Temperature		A Hybrid Power Amplifier Using 3-Phase 3-		Thermally Stable Integrated Se Deced OTS	Colorton with > 20 MA/and ² Current Drive > 2 40 ³ Lloff Disc	Linix of	A Powerless and Non-Volatile Counterfeit IC
	Minnesota Minnesota	System	Compensated CMOS On-Chip Oscillator	KAIST	Level Class-D with 200nH Inductors and	imec	Nonlinearity, Tunable Threshold Voltage and	Excellent Endurance	Univ. of Detection Sensor in a Standard Logic Process	
	IES1 3 11:20 11:45	C10.3	Using Voltage Ratio Adjusting Technique	C11 3	Current Balancing Technique	T7 3	11:20 11:45		Based on an Exposed Floating-Gate Array	
10:30-12:35	Future / Vuture and Noise Margin Impacts of Aging on Doming	0.000	An 8GHz, 0.005mm ² All Digital Clock	The Univ.		11.0		The shall be the site for black Orithmer Deadler Orientian	0	An All Pixel PDAE CMOS Image Sensor with 0.64um×1.26
	Intel Read, Static Write, and Retention of 8T 1R1W SRAM	Samsung Electronics	Generator Having 0.1% Frequency	of Texas	A 1V 0.25uW Inverter-Stacking Amplifier with 1.07 Noise Efficiency Factor	CEA-LETI	Innovative PCM+01S Device with High Sub and Higher Endurance Performance	- I hreshold Non-Linearity for Non-Switching Reading Operations	Samsung	μm Photodiode Separated by Self-Aligned In-Pixel Deep
	Arrays in 22nm High-k/Metal-Gate Tri-Gate CMOS	C10.4	Accuracy by New ZTC Algorithm	at Austin	11.45 12.40	T7 4	11.45 10:40		T0 4	14:45 42:40
	JFS1-4 11.45-12.10 National Excellent Reliability of Ferroelectric HfZrO	010-4	A 4GHz Clock Distribution Architecture Using	011-4	11.45-12.10	17-4	11:45-12:10		10-4	11.45-12.10
	Tsing Hua Free from Wake-Up and Fatigue Effects b	TSMC	Subharmonically Injection-Locked Coupled	Univ. of	A 150-µW 3 rd -Order Butterworth Passive-	Samsung	A Novel Write Method for Improving RESET	Distribution of PRAM	Hitachi	FET-Type Hydrogen Sensor with Short
	Univ. NH ₃ Plasma Treatment		CMOS	TOPOPILO	Switched-Capacitor Filter with 92 dB SFDR	Electronics				Response Time and High Drift Infindrity
	JFS1-5 12:10-12:35	C10-5	12:10-12:35	C11-5	12:10-12:35	-				
	of Texas Power Driver with Closed-Loop Adaptive	Taiwan	A 5.12-GHz Fractional-N Frequency	KAIST	Voltage Reference with PSRR of -81dB and					
	at Dallas Miller Plateau Sensing	Univ.	Synthesizer with an LC-VCO-Based MDLL		Line Sensitivity of 51ppm/V in 0.18um CMOS					
12:35-14:00										
12:35-14:00	IEO0: Advanced Accembly		40. CDAM & Emersion Memory	040. Die	-invest Descending / Manitaging Observite		70.0			T40: D-li-Lillo
12:35-14:00	JFS2: Advanced Assembly	C12-1	12: SRAM & Emerging Memory	C13: Bio C13-1	signal Recording / Monitoring Circuits	T9-1	T9: S	iGe/Ge FET 1	T10-1	T10: Reliability
12:35-14:00	JFS2: Advanced Assembly JFS2-1 14:00-14:25 A Dialally Controlled Fully Interacted Vallage Regulator	C C12-1	12: SRAM & Emerging Memory 14:00-14:25 A 31.2pJ/disparity-pixel Stereo Matching	C13: Bio C13-1	signal Recording / Monitoring Circuits 14:00-14:25 3.37 µW/Ch Modular Scalable Neural	T9-1	T9: S 14:00-14:25	iGe/Ge FET 1	T10-1	T10: Reliability 14:00-14:25
12:35-14:00	JFS2: Advanced Assembly JFS2-1 14:00-14:25 A Digitally Controlled Fully Integrated Votage Regulator with 30-T5V Based On-Die Sciencial Inductor with Bactiside Blazed Mandel Core in Ideator 10:54 act OMO-	C12-1 KAIST	12: SRAM & Emerging Memory 14:00-14:25 A 31.2pJ/disparity-pixel Stereo Matching Processor with Stereo SRAM for Mobile UI	C13: Bio C13-1 Univ. of Michigan	signal Recording / Monitoring Circuits 14:00-14:25 3:37 µW/Ch Modular Scalable Neural Recording System with Embedded Lossless	T9-1 IBM Research	T9: S 14:00-14:25 High Performance and Record Subthreshold Ge-Content Channels Formed by 3D Conder	iGe/Ge FET 1 Swing Demonstration in Scaled RMG SiGe FinFETs with High- sation and a Novel Gate Stack Process	T10-1 TSMC	T10: Reliability 14:00-14:25 On-Die 16nm Metal Critical Peak Current Test Methodology with 100ps Pulse Width
12:35-14:00	JFS2: Advanced Assembly JFS2-1 14:00-14:25 A Dipitally Controlled Fully Integrated Voltage Regulator with 3D-TSV Based On-Die Schmid Inductor with Backside Planar Magnetic Core in 14nm Tri-Gate CMOS IFS2-2 14:25-14:50	C12-1 KAIST	12: SRAM & Emerging Memory 14:00-14:25 A 31.2pJ/disparity pixel Stereo Matching Processor with Stereo SRAM for Mobile UI Application 14:25-14:50	C13: Bio C13-1 Univ. of Michigan	signal Recording / Monitoring Circuits 14:00-14:25 3.37 µW/Ch Modular Scalable Neural Recording System with Embedded Lossless Compression for Dynamic Power Reduction 14:25-14:50	T9-1 IBM Research	T9: 5 14:00-14:25 High Performance and Record Subtrreshold Ge-Content Channels Formed by 3D Conder 14:25-14:50	iGe/Ge FET 1 Swing Demonstration in Scaled RMG SiGe FinFETs with High- sation and a Novel Gate Stack Process	T10-1 TSMC	T10: Reliability 14:00-14:25 On-Die 16mm Metal Critical Peak Current Test Methodology with 100ps Pulse Width 14:25.14:50
12:35-14:00	JFS2: Advanced Assembly JFS2-1 14:00-14:25 A Digitally Controlled Fully Integrated Voltage Regulator Intel with 3D-TSV Based On-Die Sciendo Inductor with Backside Planar Magnetic Core in 14rm Tri-Gate CMOS JFS2-2 14:25-14:50 A 6Gb/s Rotatable Non-Contact Connector	C12-1 KAIST C12-2	12: SRAM & Emerging Memory 14:00-14:25 A 31.2pJ/disparity-pixel Stereo Matching Processor with Stereo SRAM for Mobile UI Application 14:26-14:50 A 0.3V VDDmin 4+2T SRAM for Searching.	C13: Bio C13-1 Univ. of Michigan C13-2	signal Recording / Monitoring Circuits 14:00-14:25 3.37 µW/Ch Modular Scalable Neural Recording System with Embedded Lossless Compression for Dynamic Power Reduction 14:25-14:50	T9-1 IBM Research T9-2	T9: S 14:00-14:25 High Performance and Record Subthreshold Ge-Content Channels Formed by 3D Conder 14:25-14:50	iGe/Ge FET 1 Swing Demonstration in Scaled RMG SiGe FinFETs with High- isation and a Novel Gate Stack Process	T10-1 TSMC T10-2	T10: Reliability 14:00-14:25 On-Die 16nm Metal Critical Peak Current Test Methodology with 100ps Pulse Width 14:25-14:50
12:35-14:00	JFS2: Advanced Assembly JFS2-1 14:00-14:25 A Digitally Controlled Fully Integrated Votage Regulator Intel with 3D-TSV Baed On-Die Schend Inducer with Backside Planar Magnetic Core in 14nm Tri-Gate CMOS JFS2-2 14:25-14:50 A 6Gb/s Rotatable Non-Contact Connector Keio Univ. with High-Speed/I ² C/CAN/SPI Interface	C12-1 KAIST C12-2 Univ. of Michigan	12: SRAM & Emerging Memory 14:00-14:25 A 31 2pJ/disparity-pixel Stereo Matching Processor with Stereo SRAM for Mobile UI Application 14:25-14:50 A 0.3V VDDmin 4+2T SRAM for Searching and In-Memory Computing Using 55nm	C13: Bio C13-1 Univ. of Michigan C13-2 imec/Holst Centre	signal Recording / Monitoring Circuits 14:00-14:25 3.37 µW/Ch Modular Scalable Neural Recording System with Embedded Lossless Compression for Dynamic Power Reduction 14:25-14:50 A 36µW Reconfigurable Analog Front-End IC for Multimodal Vital Signs Monitoring	T9-1 IBM Research T9-2 IBM Research	T9: S 14:00-14:25 High Performance and Record Subhreshold Ge-Content Channels Formed by 3D Conder 14:25-14:50 SiGe FinFET for Practical Logic Libraries by	iGe/Ge FET 1 Swing Demonstration in Scaled RMG SiGe FinFETs with High- isation and a Novel Gate Stack Process Mitigating Local Layout Effect	T10-1 TSMC T10-2 KU Leuver	T10: Reliability 14:00-14:25 On-Die 16nm Metal Critical Peak Current Test Methodology with 100ps Pulse Width 14:25-14:50 A Fully-Integrated Method for RTN Parameter Extraction
<u>12:35-14:00</u> 14:00-15:40	JFS2: Advanced Assembly JFS2-1 14:00-14:25 A Digitally Centrolide Fully Integrated Voltage Regulator with 30-375V Band On-Die Sciencil Inductor with Band On-Die Sciencil Inductor with JFS2-2 14:25-14:50 A 65D/s Rotatable Non-Contact Connector Keio Univ. with High-Speed/ ² C/CAN/SPI Interface Bridge IC.	C12-1 KAIST C12-2 Univ. of Michigan	12: SRAM & Emerging Memory 14:00-14:25 A 31 2pJ/disparity-pixel Stereo Matching Processor with Stereo SRAM for Mobile UI Application 14:25-14:50 A 0.3V VDDmin 4+2T SRAM for Searching and In-Memory Computing Using 55nm DDC Technology	C13: Bio C13-1 Univ. of Michigan C13-2 imec/Holst Centre	signal Recording / Monitoring Circuits 14:00-14:25 3.37 JW/Ch Modular Scalable Neural Recording System with Embedded Lossless Compression for Dynamic Power Reduction 14:25-14:50 A 36JW Reconfigurable Analog Front-End IC for Multimodal Vital Signs Monitoring	T9-1 IBM Research T9-2 IBM Research	T9: 5 14:00-14:25 High Performance and Record Subthreshold Ge-Content Channels Formed by 3D Conder 14:25-14:50 SiGe FinFET for Practical Logic Libraries by	iGe/Ge FET 1 Swing Demonstration in Scaled RMG SiGe FinFETs with High- isation and a Novel Gate Stack Process Mitigating Local Layout Effect	T10-1 TSMC T10-2 KU Leuver	T10: Reliability 14:00-14:25 On-Die 16nm Metal Critical Peak Current Test Methodology with 100ps Pulse Width 14:25-14:50 A Fully-Integrated Method for RTN Parameter Extraction 44:50.654.5
<u>12:35-14:00</u> 14:00-15:40	JFS2: Advanced Assembly JFS2-1 14:00-14:25 A Digitally Controlled Fully Integrated Voltage Regulator with 30-159 Based On-Die Schenol Inductor with Backetake Planar Magnetic Care In 14mm Tr-Gate CMOS JFS2-2 14:25-14:50 A 6Gb/s Rotatable Non-Contact Connector Keio Univ. With High-Speed/I ² C/CAN/SPI Interface Bridge IC JFS2-3 14:50-15:15	C12-1 KAIST C12-2 Univ. of Michigan C12-3 Semicondu	12: SRAM & Emerging Memory 14:00-14:25 A 31 2pJ/disparity pixel Stereo Matching Processor with Stereo SRAM for Mobile UI Application 14:25-14:50 A 0.3V VDDmin 4+2T SRAM for Searching and In-Memory Computing Using 55nm DDC Technology 14:50-15:15	C13: Bio C13-1 Univ. of Michigan C13-2 imec/Holst Centre C13-3	signal Recording / Monitoring Circuits 14:00-14:25 3.37 W/Ch Modular Scalable Neural Recording System with Embedded Lossless Compression for Dynamic Power Reduction 14:25-14:50 A 36µW Reconfigurable Analog Front-End IC for Multimodal Vital Signs Monitoring 14:50-15:15 A Scalable LichbuMultiniewed Delta-Encoded Distal	T9-1 IBM Research T9-2 IBM Research T9-3	T9: 5 14:00-14:25 High Performance and Record Subthreshold Ge-Content Channels Formed by 3D Conder 14:25-14:50 SiGe FinFET for Practical Logic Libraries by 14:50-15:15	iGe/Ge FET 1 Swing Demonstration in Scaled RMG SiGe FinFETs with High- isation and a Novel Gate Stack Process Mitigating Local Layout Effect	T10-1 TSMC T10-2 KU Leuver T10-3	T10: Reliability 14:00-14:25 On-Die 16nm Metal Critical Peak Current Test Methodology with 100ps Pulse Width 14:25-14:50 A Fully-Integrated Method for RTN Parameter Extraction 14:50-15:15 New Insight on the Geometry Dependence.
<u>12:35-14:00</u> 14:00-15:40	JFS2: Advanced Assembly JFS2-1 14:00-14:25 A Digitally Controlled Fully Integrated Voltage Regulator with 30-15V Based On-Die Schenol Inductor with Backsice Planer Magnetic Core in 14em Tri-Gate CMOS JFS2-2 14:25-14:50 A 6Gb/s Rotatable Non-Contact Connector Keio Univ. with High-Speed// ² C/CAN/SPI Interface Bridge IC JFS2-3 14:50-15:15 High Density 3D Fanout Package for High Density 3D Fanout Package for	C12-1 KAIST C12-2 Univ. of Michigan C12-3 Semicondu ctor Energy	12: SRAM & Emerging Memory 14:00-14:25 A 31.2pJ/disparity pixel Stereo Matching Processor with Stereo SRAM for Mobile UI Application 14:25-14:50 A 0.3V VDDmin 4+2T SRAM for Searching and In-Memory Computing Using 55nm DDC Technology 14:50-15:15 A 140 MHz 1 Mbit 2T1C Gain-Cell Memory with 60-m Indium-Gallium-Zin Coxder Transistor Embedded Into 65-	C13: Bio C13-1 Univ. of Michigan C13-2 imec/Holst Centre C13-3 Univ. of Washington	signal Recording / Monitoring Circuits 14:00-14:25 3.37 µW/Ch Modular Scalable Neural Recording System with Embedded Lossless Compression for Dynamic Power Reduction 14:25-14:50 A 36µW Reconfigurable Analog Front-End IC for Multimodal Vital Signs Monitoring 14:50-15:15 A Scalable, Highly-Multiplexed Deta-Encoded Digital Feedback ECoG Recording Amplifier with Common	T9-1 IBM Research T9-2 IBM Research T9-3 The Univ.	T9: 5 14:00-14:25 High Performance and Record Subtrreshold Ge-Content Channels Formed by 3D Conder 14:25-14:50 SiGe FinFET for Practical Logic Libraries by 14:50-15:15 High Performance 4.5-nm-Thick Compressive Condensation with Optimized Temperature	iGe/Ge FET 1 Swing Demonstration in Scaled RMG SiGe FinFETs with High- isation and a Novel Gate Stack Process Mitigating Local Layout Effect	T10-1 TSMC T10-2 KU Leuver T10-3 CEA-LETI	T10: Reliability 14:00-14:25 On-Die 16mm Metal Critical Peak Current Test Methodology with 100ps Pulse Width 14:25-14:50 A Fully-Integrated Method for RTN Parameter Extraction 14:50-15:15 New Insight on the Geometry Dependence of BTI in 3D Technologies Based on
<u>12:35-14:00</u> 14:00-15:40	JFS2: Advanced Assembly JFS2-1 14:00-14:25 A Diplatily Controlled Fully Integrated Voltage Regulator Intel with 3D-TSV Based On-Die Sciencel Inducer with Backside Planar Magnetic Core in 14rm Tri-Gate CMOS JFS2-2 14:25-14:50 A 6Gb/s Rotatable Non-Contact Connector Keio Univ. with High-Speed/I ² C/CAN/SPI Interface Bridge IC JFS2-3 14:50-15:15 TSMC High Density 3D Fanout Package for Heterogeneous Integration	C12-1 KAIST C12-2 Univ. of Michigan C12-3 Semicondu ctor Energy Laboratory	12: SRAM & Emerging Memory 14:00-14:25 A 31.2pJ/disparity-pixel Stereo Matching Processor with Stereo SRAM for Mobile UI Application 14:25-14:50 A 0.3V VDDmin 4+2T SRAM for Searching and In-Memory Computing Using 55nm DDC Technology 14:50-15:15 A 140 MHz 1 Mbit 2TI Clair-Cell Memory with 60-m IndumGallim-Zinc Oxder Transistor Embedded Into 65- nm CMOS Logic Process Technology	C13: Bio C13-1 Univ. of Michigan C13-2 imec/Holst Centre C13-3 Univ. of Washington	signal Recording / Monitoring Circuits 14:00-14:25 3.37 μW/Ch Modular Scalable Neural Recording System with Embedded Lossless Compression for Dynamic Power Reduction 14:25-14:50 A 36μW Reconfigurable Analog Front-End IC for Multimodal Vital Signs Monitoring 14:50-15:15 A Saabe, Highly-Multiplexed Delta-Encoded Digital Feedback EcoG Recording Amplifier with Common and Differential-Mode Artifact Suppression	T9-1 IBM Research T9-2 IBM Research T9-3 The Univ. of Tokyo	T9: 5 14:00-14:25 High Performance and Record Subthreshold Ge-Content Channels Formed by 3D Conder 14:25-14:50 SiGe FinFET for Practical Logic Libraries by 14:50-15:15 High Performance 4.5-nm-Thick Compressiv Condensation with Optimized Temperature C	iGe/Ge FET 1 Swing Demonstration in Scaled RMG SiGe FinFETs with High- isation and a Novel Gate Stack Process Mitigating Local Layout Effect ely-Strained Ge-On-Insulator pMOSFETs Fabricated by Ge Control	T10-1 TSMC T10-2 KU Leuver T10-3 CEA-LETI	T10: Reliability 14:00-14:25 On-Die 16nm Metal Critical Peak Current Test Methodology with 100ps Pulse Width 14:25-14:50 A Fully-Integrated Method for RTN Parameter Extraction 14:50-15:15 New Insight on the Geometry Dependence of BTT in 3D Technologies Based on Experiments and Modeling
<u>12:35-14:00</u> 14:00-15:40	JFS2: Advanced Assembly JFS2-1 14:00-14:25 A Digitally Controlled Fully Integrated Voltage Regulator Intel with 3D-TSV Based On-Die Sciendel Inductor with Backside Planar Magnetic Core in 14rm Tri-Gate CMOS JFS2-2 14:25-14:50 A 6Gb/s Rotatable Non-Contact Connector Keio Univ. with High-Speed/I ² C/CAN/SPI Interface Bridge IC JFS2-3 14:50-15:15 TSMC High Density 3D Fanout Package for Heterogeneous Integration JFS2-4 15:15:15:40	C12-1 KAIST C12-2 Univ. of Michigan C12-3 Semicondu ctor Energy Laboratory C12-4 National	12: SRAM & Emerging Memory 14:00-14:25 A 31.2pJ/disparity-pixel Stereo Matching Processor with Stereo SRAM for Mobile UI Application 14:25-14:50 A 0.3V VDDmin 4+2T SRAM for Searching and In-Memory Computing Using 55nm DDC Technology 14:50-15:15 A 140 MHz 1 Mid 2TI C Gain-Cell Memory with 60-m Indium-Galling-Zin Cell Memory with 60-m m CMOS Logic Process Technology 15:15-15:40	C13: Bio C13-1 Univ. of Michigan C13-2 imec/Holst Centre C13-3 Univ. of Washington C13-4	signal Recording / Monitoring Circuits 14:00-14:25 3.37 µW/Ch Modular Scalable Neural Recording System with Embedded Lossless Compression for Dynamic Power Reduction 14:25-14:50 A 36µW Reconfigurable Analog Front-End IC for Multimodal Vital Signs Monitoring 14:50-15:15 A Scalable, Highty-Multiplexed Delta-Encoded Digital Feedback ECG Recording Amplifier with Common and Differential-Mode Artifact Suppression 15:15-15:40 B BioLingedance Readow 10 with	T9-1 IBM Research IBM Research T9-3 The Univ. of Tokyo T9-4	T9: 5 14:00-14:25 High Performance and Record Subthreshold Ge-Content Channels Formed by 3D Conder 14:25-14:50 SiGe FinFET for Practical Logic Libraries by 14:50-15:15 High Performance 4.5-nm-Thick Compressiv Condensation with Optimized Temperature O 15:15-15:40	iGe/Ge FET 1 Swing Demonstration in Scaled RMG SiGe FinFETs with High- isation and a Novel Gate Stack Process Mitigating Local Layout Effect ely-Strained Ge-On-Insulator pMOSFETs Fabricated by Ge Control	T10-1 TSMC T10-2 KU Leuver T10-3 CEA-LETI T10-4	T10: Reliability 14:00-14:25 On-Die 16nm Metal Critical Peak Current Test Methodology with 100ps Pulse Width 14:25-14:50 A Fully-Integrated Method for RTN Parameter Extraction 14:50-15:15 New Insight on the Geometry Dependence of BTI in 3D Technologies Based on Experiments and Modeling 15:15-15:40
<u>12:35-14:00</u> 14:00-15:40	JFS2: Advanced Assembly JFS2-1 14:00-14:25 A Digitally Controlled Fully Integrated Voltage Regulator with 3D-TSV Baed On-De Science Inductor with Backside Planar Megnetic Core in 14nm Tri-Gate CMOS JFS2-2 14:25-14:50 A 6Gb/s Rotatable Non-Contact Connector Keio Univ. with High-Speed/I ² C/CAN/SPI Interface Bridge IC JFS2-3 14:50-15:15 TSMC High Density 3D Fanout Package for Heterogeneous Integration JFS2-4 15:15-15:40 A Shutter-Less Micro-Bolometer Thermal Imaging SkIST System Using Multiple Digital Correlated Double	C12-1 KAIST C12-2 Univ. of Michigan C12-3 Semicondu ctor Energy Laboratory C12-4 National Tsing Hua	12: SRAM & Emerging Memory 14:00-14:25 A 31.2pJ/disparity-pixel Stereo Matching Processor with Stereo SRAM for Mobile UI Application 14:25-14:50 A 0.3V VDDmin 4+2T SRAM for Searching and In-Memory Computing Using 55nm DDC Technology 14:50-15:15 A 140 MHz 1 Mbit Z11C Gain-Cell Memory with 60-m Indum-Gailum-Znc Oxide Transistor Embedded Into 65- m OXOS Logic Process Technology 15:15-15:40 Embedded 2Nb ReRAM Macro with 2.6n Read Access Embedded ZNb ReRAM Macro with 2.6n Read Access	C13: Bio C13-1 Univ. of Michigan C13-2 imec/Holst Centre C13-3 Univ. of Washington C13-4 imec/Holst	signal Recording / Monitoring Circuits 14:00-14:25 3.37 µW/Ch Modular Scalable Neural Recording System with Embedded Lossless Compression for Dynamic Power Reduction 14:25-14:50 A 36µW Reconfigurable Analog Front-End IC for Multimodal Vital Signs Monitoring 14:50-15:15 A Scalable, Highly-Multiplexed Delta-Encoded Digital Feedback ECoG Recording Amplifier with Common and Differential-Mode Artfact Suppression 15:15-15:40 A Bio-Impedance Readout IC with Frequency Sweeping from 1k-to-1MHz for	T9-1 IBM Research T9-2 IBM Research T9-3 The Univ. of Tokyo T9-4 IBM	T9: 5 14:00-14:25 High Performance and Record Subthreshold Ge-Content Channels Formed by 3D Conder 14:25-14:50 SIGE FinFET for Practical Logic Libraries by 14:50-15:15 High Performance 4.5-nm-Thick Compressiv Condensation with Optimized Temperature 0 15:15-16:40 Understanding the Interfacial Layer Formatic	iGe/Ge FET 1 Swing Demonstration in Scaled RMG SiGe FinFETs with High- isation and a Novel Gate Stack Process Mitigating Local Layout Effect ely-Strained Ge-On-Insulator pMOSFETs Fabricated by Ge control n on Strained Si _{1.x} Ge _x Channels and Their Correlation to Inversion	T10-1 TSMC T10-2 KU Leuver T10-3 CEA-LETI T10-4 Peking	T10: Reliability 14:00-14:25 On-Die 16nm Metal Critical Peak Current Test Methodology with 100ps Pulse Width 14:25-14:50 A Fully-Integrated Method for RTN Parameter Extraction 14:50-15:15 New Insight on the Geometry Dependence of BT1 in 3D Technologies Based on Experiments and Modeling 15:15-15:40 Unified Self-Heating Effect Model for Advanced Digital and Analog Technology and Thermal-
12:35-14:00	JFS2: Advanced Assembly JFS2-1 14:00-14:25 A Digitally Controlled Fully Integrated Values Regulator intel with 3D-TSV Based On-De School Inductor with Backside Planar Magnetic Core in 14cm Tri-Gate CMOS JFS2-2 14:25-14:50 A 66D/s Rotatable Non-Contact Connector Keio Univ. with High-Speed/ ¹² C/CAN/SPI Interface Bridge IC JFS2-3 14:50-15:15 TSMC High Density 3D Fanout Package for Heterogeneous Integration JFS2-4 15:15-15:40 A Shutter-Less Micro-Bolometer Thermal Imaging System Using Multiple Digital Correlated Double Sampling for Mobile Applications	C12-1 C12-1 KAIST C12-2 Univ. of Michigan C12-3 Semicondu tor Energy Laboratory C12-4 National Tsing Hua Univ.	12: SRAM & Emerging Memory 14:00-14:25 A 31 2pJ/disparity pixel Stereo Matching Processor with Stereo SRAM for Mobile UI Application 14:25-14:50 A 0.3V VDDmin 4+2T SRAM for Searching and In-Memory Computing Using 55nm DDC Technology 14:50-15:15 A 140 Mit: 1 Mbit 2T IC Gain-Cell Memory with 60-m Indium-Gallium-Zinc Oxide Transistor Embedded Into 65- nm CMOS Loige Process Technology 15:15-15:40 Embedded 2Mb ReRAM Macro with 2.6 ns Read Access Time Using Dynamic-Tinp-Pointhematch Samping Current-Mode Sense Amplifier for IcE Applications	C13: Bio C13-1 Univ. of Michigan C13-2 imec/Holst Centre C13-3 Univ. of Washington C13-4 imec/Holst Centre	signal Recording / Monitoring Circuits 14:00-14:25 3.37 µW/Ch Modular Scalable Neural Recording System with Embedded Lossless Compression for Dynamic Power Reduction 14:25-14:50 A 36µW Reconfigurable Analog Front-End IC for Multimodal Vital Signs Monitoring 14:50-15:15 A Scalable, Highly-Multiplexed Delta-Encoded Digital Feedback ECoG Recording Amplifier with Common and Differential-Mode Artifact Suppression 15:15-15:40 A Bio-Impedance Readout IC with Frequency Sweeping from 1k-to-1MHz for Electrical Impedance Tomography	T9-1 IBM Research T9-2 IBM Research T9-3 The Univ. of Tokyo T9-4 IBM Research	T9: 5 14:00-14:25 High Performance and Record Subhreshold Ge-Content Channels Formed by 3D Conder 14:25-14:50 SiGe FinFET for Practical Logic Libraries by 14:50-15:15 High Performance 4.5-nm-Thick Compressiv Condensation with Optimized Temperature O 15:15-15:40 Understanding the Interfacial Layer Formatic Layer Hole Mobility	iGe/Ge FET 1 Swing Demonstration in Scaled RMG SiGe FinFETs with High- isation and a Novel Gate Stack Process Mitigating Local Layout Effect ely-Strained Ge-On-Insulator pMOSFETs Fabricated by Ge control n on Strained Si _{1-x} Ge _x Channels and Their Correlation to Inversion	T10-1 TSMC T10-2 KU Leuver T10-3 CEA-LETI T10-4 Peking Univ.	T10: Reliability 14:00-14:25 On-Die 16nm Metal Critical Peak Current Test Methodology with 100ps Pulse Width 14:25-14:50 A Fully-Integrated Method for RTN Parameter Extraction 14:50-15:15 New Insight on the Geometry Dependence of BT in 3D Technologies Based on Experiments and Modeling 15:15-15:40 Unified Self-Heating Effect Model for Advanced Digital and Analog Technology and Thermal- Aware Lifetime Prediction Methodology
12:35-14:00	JFS2: Advanced Assembly JFS2-1 14:00-14:25 A Digitally Controlled Fully Integrated Voltage Regulator with 3D-TSV Based No-De School Inductor with Backside Planar Magnetic Core in 14rm Tri-Gate CMOS JFS2-2 14:25-14:50 A 6Gb/s Rotatable Non-Contact Connector Keio Univ. with High-Speed/ ¹² C/CAN/SPI Interface Bridge IC JFS2-3 14:50-15:15 TSMC High Density 3D Fanout Package for Heterogeneous Integration JFS2-4 15:15-15:40 XAIST Samp Multipe Digital Correlated Double Sampling for Mobile Applications C14: Phase-Locked Loops	C12-1 C12-1 KAIST C12-2 Univ. of Michigan C12-3 Semicondu ctor Energy Laboratory C12-4 National Tsing Hua Univ. C15: 1	12: SRAM & Emerging Memory 14:00-14:25 A 31 2pJ/disparity-pixel Stereo Matching Processor with Stereo SRAM for Mobile UI Application 14:25-14:50 A 0.3V VDDmin 4+2T SRAM for Searching and In-Memory Computing Using 55nm DDC Technology 14:50-15:15 A 140 Mit 1 Mit 2T IC Gain-Cell Memory with 60-m Indium-Gailum-Zinc Oxide Transistor Embedded Into 65- m CMOS Logic Process Technology 15:15-15:40 Embedded 2Mb ReRAM Merro with 26 ms Read Access Imm Leing Dynamic-Tip-PointMentath Sampling Current-Mode Sense Amplifier for IcE Applications August 14:00-15:15	C13: Bio C13-1 Univ. of Michigan C13-2 imec/Holst Centre C13-3 Univ. of Washington C13-4 imec/Holst Centre C	signal Recording / Monitoring Circuits 14:00-14:25 3.37 µW/Ch Modular Scalable Neural Recording System with Embedded Lossless Compression for Dynamic Power Reduction 14:25-14:50 A 36µW Reconfigurable Analog Front-End IC for Multimodal Vital Signs Monitoring 14:50-15:15 A Scalable, Highy-Multiplexed Delta-Encoded Digital Feedback ECoG Recording Amplifier with Common and Differential-Mode Artifact Suppression 15:15-15:40 A Bio-Impedance Readout IC with Frequency Sweeping from Ik-to-1MHz for Electrical Impedance Tomography 16: Power Management Circuit	T9-1 IBM Research T9-2 IBM Research T9-3 The Univ. of Tokyo T9-4 IBM Research	T9: 5 14:00-14:25 High Performance and Record Subthreshold Ge-Content Channels Formed by 3D Conder 14:25-14:50 SiGe FinFET for Practical Logic Libraries by 14:50-15:15 High Performance 4.5-nm-Thick Compressiv Condensation with Optimized Temperature C 15:15-15:40 Understanding the Interfacial Layer Formatic Layer Hole Mobility T11: CN	iGe/Ge FET 1 Swing Demonstration in Scaled RMG SiGe FinFETs with High- isation and a Novel Gate Stack Process Mitigating Local Layout Effect ely-Strained Ge-On-Insulator pMOSFETs Fabricated by Ge control n on Strained Si _{1-a} Ge _x Channels and Their Correlation to Inversion IOS Integration 1	T10-1 TSMC T10-2 KU Leuver T10-3 CEA-LETI T10-4 Peking Univ.	T10: Reliability 14:00-14:25 On-Die 16nm Metal Critical Peak Current Test Methodology with 100ps Pulse Width 14:25-14:50 A Fully-Integrated Method for RTN Parameter Extraction 14:50-15:15 New Insight on the Geometry Dependence of BT1 in 3D Technologies Based on Experiments and Modeling 5:15-15:40 Unified Self-Heating Effect Model for Advanced Digital and Analog Technology and Thermal- ware Lifetime Prediction Methodology 112: Ferroelectric
12:35-14:00	JFS2: Advanced Assembly JFS2-1 14:00-14:25 A Digitally Controlled Fully Integrated Votage Regulator With With 37:5V Baach On-Die Sciencil Ordecce with Backside Planar Magnetic Core in 14nm Tri-Gate CMOS JFS2-2 14:25-14:50 A 6Gb/s Rotatable Non-Contact Connector Keid Univ. with High-Speed/I ² C/CAN/SPI Interface Bridge IC JFS2-3 14:50-15:15 TSMC High Density 3D Fanout Package for Heterogeneous Integration JFS2-4 15:15-15:40 A Shutter-Less Micro-Bolometer Thermal Imaging System Using Multiple Digital Corelated Double Sampling for Mobile Applications C14: Phase-Locked Loops C14-1 16:00-16:25	C12-1 KAIST C12-2 C12-2 Univ. of Michigan C12-3 Semicondu ctor Energy Laboratory C12-4 National Tsing Hua Univ. C15-1	12: SRAM & Emerging Memory 14:00-14:25 A 31.2pJ/disparity pixel Stereo Matching Processor with Stereo SRAM for Mobile UI Application 14:25-14:50 A 0.3V VDDmin 4+2T SRAM for Searching and In-Memory Computing Using 55nm DDC Technology 14:50-15:15 A 140 MHz 1 Mbit 2T1 CGan-Cell Memory with 60-m fidumGalius-Znc Oxide Transitor Embedded Into 65- m GMOS Logic Process Technology 15:15-15:40 Enbedded 2Mb RRAM Macro with 2.6n Read Access Time Using Dynamic-Tip-Point-Mematch Sampling Current-Mode Sense Applifer for UE Applications Memory Interface and Flash Memory 16:00-16:25	C13: Bio C13-1 Univ. of Michigan C13-2 imec/Holst Centre C13-3 Univ. of Washington C13-4 imec/Holst Centre C16-1	signal Recording / Monitoring Circuits 14:00-14:25 3.37 µW/Ch Modular Scalable Neural Recording System with Embedded Lossless Compression for Dynamic Power Reduction 14:25-14:50 A 36µW Reconfigurable Analog Front-End Ic for Multimodal Vital Signs Monitoring 14:50-15:15 A Scalable, Highly-Multiplexed Delta-Encoded Digital Feedback ECoG Recording Amplifier with Common and Differential-Mode Artifact Suppression 15:15-15:40 A Bio-Impedance Readout IC with Frequency Sweeping from 1k-to-1MHz for Electrical Impedance Tomography 16: Power Management Circuit 16:00-16:25 A 1452% Power Estraction Improvement Energy	T9-1 IBM Research T9-2 IBM Research T9-3 The Univ. of Tokyo T9-4 IBM Research T11-1	T9: 5 14:00-14:25 High Performance and Record Subtrreshold Ge-Content Channels Formed by 3D Conder 14:25-14:50 SiGe FinFET for Practical Logic Libraries by 14:50-15:15 High Performance 4.5-nm-Thick Compressiv Condensation with Optimized Temperature C 15:15-15:40 Understanding the Interfacial Layer Formatic Layer Hole Mobility T11: CM 16:00-16:25	iGe/Ge FET 1 Swing Demonstration in Scaled RMG SiGe FinFETs with High- isation and a Novel Gate Stack Process Mitigating Local Layout Effect ely-Strained Ge-On-Insulator pMOSFETs Fabricated by Ge Sontrol n on Strained Si _{1-x} Ge _x Channels and Their Correlation to Inversion IOS Integration I	T10-1 TSMC T10-2 KU Leuver T10-3 CEA-LETI T10-4 Peking Univ.	T10: Reliability 14:00-14:25 On-Die 16mm Metal Critical Peak Current Test Methodology with 100ps Pulse Width 14:25-14:50 A Fully-Integrated Method for RTN Parameter Extraction 14:50-15:15 New Insight on the Geometry Dependence of BTI in 3D Technologies Based on Experiments and Modeling 15:15-15:40 Unified Self-Heating Effect Model for Advanced Digital and Analog Technology and Thermal- Aware Lifetime Prediction Methodology T12: Ferroelectric 16:00-16:25
12:35-14:00	JFS2: Advanced Assembly JFS2-1 14:00-14:25 A Diplatify Controlled Fully Integrated Voltage Regulator With 3D-TSV Based On-Die Sciend Inductor with Backside Planar Magnetic Core in 14rm Tri-Gate CMOS JFS2-2 14:25-14:50 A 6Gb/s Rotatable Non-Contact Connector Keio Univ. with High-Speed/I ² C/CAN/SPI Interface Bridge IC JFS2-3 14:50-15:15 TSMC High Density 3D Fanout Package for Heterogeneous Integration JFS2-4 15:15-15:40 A Shutter-Less Micro-Bolometer Thermal Imaging System Using Multiple Digital Correlated Double Sampling for Mobile Applications C14-1 16:00-16:25 A 0.5V 16mW 2.4GHz Fractional-N Al-Digital PLL TSMC for Buletooth LE with PVT-Insensity TD C Using	C12-1 KAIST C12-2 Univ. of Michigan C12-3 Semicondu ctor Energy Laboratory C12-4 National Tsing Hua Univ. C15-1 C15-1	12: SRAM & Emerging Memory 14:00-14:25 A 31.2pJ/disparity-pixel Stereo Matching Processor with Stereo SRAM for Mobile UI Application 14:25-14:50 A 0.3V VDDmin 4+2T SRAM for Searching and In-Memory Computing Using 55nm DDC Technology 14:50-15:15 A 140 MHz 1 Mbit 2TI Clair-Cell Memory with 60-m IndumGallma-Zin Code Transitor Embedded Into 65- m CMOSL logic Process Technology 15:15-15:40 Embedded 2Mb RRAM Macro with 2 Gins Read Access Time Lising Dynamic-Tip-Point Memory Current-Mode Sense Amplifier for IcE Applications demory Interface and Flash Memory 16:00-16:25 A Floating Tap Termination Scheme with Inverted DBI AC and Floating Tap Forcing	C13: Bio C13-1 Univ. of Michigan C13-2 imec/Holst Centre C13-3 Univ. of Washington C13-4 imec/Holst Centre C16-1 KAIST	signal Recording / Monitoring Circuits 14:00-14:25 3.37 µW/Ch Modular Scalable Neural Recording System with Embedded Lossless Compression for Dynamic Power Reduction 14:25-14:50 A 36µW Reconfigurable Analog Front-End IC for Multimodal Vital Signs Monitoring 14:50-15:15 A Scalable, Highly-Multiplexed Delta-Encoded Digital Feedback ECG Recording Amplifier with Common and Differential-Mode Artifact Suppression 15:15-15:40 A Bio-Impedance Readout IC with Frequency Sweeping from 1k-to-1MHz for Electrical Impedance Tomography 16:0-16:25 A 1452-%; Power Editaction Improvement Energy Hardson Frequency Statement Energy Hardson Frequency Statement Energy A 1452-%; Power Editaction Improvement Energy Hardson Frequency Statement Energy Hardson Frequency Hardson Freq	T9-1 IBM Research T9-2 IBM Research T9-3 The Univ. of Tokyo T9-4 IBM Research T11-1 GLOBALFC	T9: 5 14:00-14:25 High Performance and Record Subthreshold Ge-Content Channels Formed by 3D Conder 14:25-14:50 SiGe FinFET for Practical Logic Libraries by 14:50-15:15 High Performance 4.5-nm-Thick Compressiv Condensation with Optimized Temperature C 15:15-15:40 Understanding the Interfacial Layer Formatic Layer Hole Mobility T11: CM 16:00-16:25 14nm FinFET Technology for Analog and RP	iGe/Ge FET 1 Swing Demonstration in Scaled RMG SiGe FinFETs with High- isation and a Novel Gate Stack Process Mitigating Local Layout Effect ely-Strained Ge-On-Insulator pMOSFETs Fabricated by Ge Control n on Strained Si _{1-a} Ge _x Channels and Their Correlation to Inversion IOS Integration 1 Applications	T10-1 TSMC T10-2 KU Leuver T10-3 CEA-LETI T10-4 Peking Univ. T12-1 National Nano Device	T10: Reliability 14:00-14:25 On-Die 16nm Metal Critical Peak Current Test Methodology with 100ps Pulse Width 14:25-14:50 A Fully-Integrated Method for RTN Parameter Extraction 14:50-15:15 New Insight on the Geometry Dependence of BTi in 3D Technologies Based on Experiments and Modeling 15:15-15:40 Unified Self-Heating Effect Model for Advanced Digital and Analog Technology and Thermal- Aware Lifetime Prediction Methodology T12: Ferroelectric 16:00-16:25 Nano-Scaled Ge FinFETs with Low Temperature Ferroelectric Interfacial Layers
12:35-14:00	JFS2: Advanced Assembly JFS2-1 14:00-14:25 A Digitally Controlled Fully Integrated Voltage Regulator with 3D-TSV Based On-De Sciend Inductor with Backside Planar Magnetic Core in 14nm Tri-Gate CMOS JFS2-2 14:25-14:50 A 650/s Rotatable Non-Contact Connector Keio Univ. A 650/s Rotatable Non-Contact Connector Bridge IC JFS2-3 14:50-15:15 TSMC High Density 3D Fanout Package for Heterogeneous Integration JFS2-4 15:15:15:40 KAIST System Using Multiple Digital Corteiated Double Sampling for Mobile Applications C14-1 16:00-18:25 C14-1 16:00-18:25 X 0.5V 1.8mW 2.4GHz Fractional-N Al-Digital PLL for Bluetont Le With PVT-Insensitive TOC Using switched-Capacitor Doubler in 28nm CMOS	C12-1 KAIST C12-2 Univ. of Michigan C12-3 Semicondu ctor Energy Laboratory C12-4 National Tsing Hua Univ. C15-1 C15-1 SK hynix	12: SRAM & Emerging Memory 14:00-14:25 A 31.2pJ/disparity pixel Stereo Matching Processor with Stereo SRAM for Mobile UI Application 14:25-14:50 A 0.3V VDDmin 4+2T SRAM for Searching and In-Memory Computing Using 55nm DDC Technology 14:50-15:15 A 140 Mkr 1 Mid 2T/C Gain-Call Memory with 60-m Indum-Gallmar-Call Calm-Call Memory with 60-m Midum-Gallmar-Call Calm Call Memory with 60-m m CMOS Logic Process Technology 15:15-15:40 Embedded 2Mb ReRAM Macro with 2.6m Read Access Time Using Dynamic-Trip-Point-Mismatch Sampling Current-Mode Sense Amplifier for IG-Applications Anory Interface and Flash Memory 16:00-16:25 A Floating Tap Termination Scheme with Inverted DBR AC and Floating Tap Forcing Technique for High-Speed Low-Power Signaling	C13: Bio C13-1 Univ. of Michigan C13-2 imec/Holst Centre C13-3 Univ. of Washington C13-4 imec/Holst Centre C13-4 KAIST	signal Recording / Monitoring Circuits 14:00-14:25 3.37 µW/Ch Modular Scalable Neural Recording System with Embedded Lossless Compression for Dynamic Power Reduction 14:25-14:50 A 36µW Reconfigurable Analog Front-End IC for Multimodal Vital Signs Monitoring 14:50-15:15 A Scalable, Highly-Multiplexed Detta-Encoded Digital Feedback ECoG Recording Amplifier with Common and Differential-Mode Artifact Suppression and Differential-Mode Artifact Suppression 15:15-15:40 A Bio-Impedance Readout IC with Frequency Sweeping from 1k-to-1MHz for Electrical Impedance Tomography 16: Power Management Circuit 16:00-16:25 A 1462% Fower Estraction Improvement Energy Harvesting Circuit Whi Simultaneous Energy Estraction from a Piezelectric Transducer and A Thermoelectric Cenerator	T9-1 IBM Research T9-2 IBM Research T9-3 The Univ. of Tokyo T9-4 IBM Research T11-1 GLOBALFC UNDRIES	T9: 5 14:00-14:25 High Performance and Record Subthreshold Ge-Content Channels Formed by 3D Conder 14:25-14:50 SiGe FinFET for Practical Logic Libraries by 14:50-15:15 High Performance 4.5-nm-Thick Compressiv Condensation with Optimized Temperature C 15:15-15:40 Understanding the Interfacial Layer Formatic Layer Hole Mobility T11: CN 16:00-16:25 14nm FinFET Technology for Analog and RF	iGe/Ge FET 1 Swing Demonstration in Scaled RMG SiGe FinFETs with High- isation and a Novel Gate Stack Process Mitigating Local Layout Effect ely-Strained Ge-On-Insulator pMOSFETs Fabricated by Ge Control n on Strained Si _{1-a} Ge _x Channels and Their Correlation to Inversion IOS Integration I Applications	T10-1 TSMC T10-2 KU Leuver T10-3 CEA-LETI T10-4 Peking Univ. T12-1 National Vano Device Laboratories	T10: Reliability 14:00-14:25 On-Die 16nm Metal Critical Peak Current Test Methodology with 100ps Pulse Width 14:25-14:50 A Fully-Integrated Method for RTN Parameter Extraction 14:50-15:15 New Insight on the Geometry Dependence of BTI in 3D Technologies Based on Experiments and Modeling 15:15-15:40 Unified Self-Heating Effect Model for Advanced Digital and Analog Technology and Thermai- Aware Lifetime Prediction Methodology T12: Ferroelectric Ferroelectric InterScal Layers Exhibiting 65% S.S. Reduction and Improved Ion
12:35-14:00	JFS2: Advanced Assembly JFS2-1 14:00-14:25 A Digitally Controlled Fully Integrated Voltage Regulator with 3D-TSV Based On-Die Sciendi Inductor with Backside Planar Magnetic Core in 14nm Tri-Gate CMOS JFS2-2 14:25-14:50 A 6Gb/s Rotatable Non-Contact Connector With High-Speed/I ² C/CAN/SPI Interface Bridge IC JFS2-3 14:50-15:15 JFS2-4 15:15-15:40 A Shutter-Less Micro-Bolometer Thermal Imaging Sampling for Mobile Applications C14:1 16:00-16:25 A 0.5V 1.8mW 2.4GH2 Fractional-N All-Digital PLL for Bluetoot LE with PVT-Insensitive TDC Using Switched-Capacitor Doubler in 28nm CMOS C14:2 16:25-16:50	C12-1 KAIST C12-2 Univ. of Michigan C12-3 Semicondu ctor Energy Laboratory C12-4 National Tsing Hua Univ. C15-1 SK hynix C15-2	12: SRAM & Emerging Memory 14:00-14:25 A 31.2pJ/disparity pixel Stereo Matching Processor with Stereo SRAM for Mobile UI Application 14:25-14:50 A 0.3V VDDmin 4+2T SRAM for Searching and In-Memory Computing Using 55nm DDC Technology 14:50-15:15 A 140 MHz 1 Mbit 2T1C Gain-Cell Memory with 60-rm IndumGallum-Zinc Oxide Transistor Embedded Into 85- nm OXOS Logic Process Technology 15:15-15:40 Embedded 2bb ReRAM Macro with 2.6m Read Access Time Using Dynamic-Tip-Point-Mismatch Sampling Current-Mode Sense Amplifer for IGE Applications Atmory Interface and Flash Memory 16:00-16:25 A Floating Tap Termination Scheme with Inverted DBI AC and Floating Tap Forcing Technique for High-Speed Low-Power Signaling 16:25-16:50	C13: Bio C13-1 Univ. of Michigan C13-2 imec/Holst Centre C13-3 Univ. of Washington C13-4 imec/Holst Centre C16-1 KAIST C16-2	signal Recording / Monitoring Circuits 14:00-14:25 3.37 µW/Ch Modular Scalable Neural Recording System with Embedded Lossless Compression for Dynamic Power Reduction 14:25-14:50 A 36µW Reconfigurable Analog Front-End IC for Multimodal Vital Signs Monitoring 14:50-15:15 A Scalable, Highly-Multiplexed Delta-Encoded Digital Feedback ECG Recording Amplifier with Common and Differential-Mode Artifact Suppression 15:15-15:40 A Bio-Impedance Readout IC with Frequency Sweeping from 1k-to-1MHz for Electrical Impedance Tomography 16:00-16:25 A 1422-19: Power Estraction Improvement Energy Harvesting Circuit With Simultaneous Energy Estraction from a Piezelectric Transducer and A Thermoelectric Generator	T9-1 IBM Research T9-2 IBM Research T9-3 The Univ. of Tokyo T9-4 IBM Research IBM Research T11-1 GLOBALFC UNDRIES T11-2	T9: 5 14:00-14:25 High Performance and Record Subthreshold Ge-Content Channels Formed by 3D Conder 14:25-14:50 SiGe FinFET for Practical Logic Libraries by 14:50-15:15 High Performance 4.5-nm-Thick Compressiv Condensation with Optimized Temperature 0 15:15-15:40 Understanding the Interfacial Layer Formatic Layer Hole Mobility T11: CM 16:00-16:25 14nm FinFET Technology for Analog and RF 16:25-16:50	iGe/Ge FET 1 Swing Demonstration in Scaled RMG SiGe FinFETs with High- isation and a Novel Gate Stack Process Mitigating Local Layout Effect ely-Strained Ge-On-Insulator pMOSFETs Fabricated by Ge Control n on Strained Si _{1.x} Ge _x Channels and Their Correlation to Inversion IOS Integration I Applications	T10-1 TSMC T10-2 KU Leuver T10-3 CEA-LETI T10-4 Peking Univ. T12-1 National Nano Device Laboratorice T12-2	T10: Reliability 14:00-14:25 On-Die 16nm Metal Critical Peak Current Test Methodology with 100ps Pulse Width 14:25-14:50 A Fully-Integrated Method for RTN Parameter Extraction 14:50-15:15 New Insight on the Geometry Dependence of BT1 in 3D Technologies Based on Experiments and Modeling 15:15-15:40 Unified Self-Heating Effect Model for Advanced Digital and Analog Technology and Thermal- Aware Lifetime Prediction Methodology T12: Ferroelectric 16:00-16:25 Nano-Scaled Ge FinFETs with Low Temperature Ferroelectric HZrO ₂ on Specific Interfacial Layers Exhibiting 65% S.S. Reduction and Improved I _{DM} 16:25-16:50
12:35-14:00	JFS2: Advanced Assembly JFS2-1 14:00-14:25 A Digitally Controlled Fully Integrated Valage Regulator with 3D-15V Based Ao-De Sciencel Inductor with Backside Planar Megnetic Care in 14mm Tri-Gate CMOS JFS2-2 14:25-14:50 A 6Gb/s Rotatable Non-Contact Connector Keio Univ. with High-Speed/l ² C/CAN/SPI Interface Bridge IC JFS2-3 14:50-15:15 TSMC High Density 3D Fanout Package for Heterogeneous Integration JFS2-4 15:15-15:40 XAStren Using Multiple Digital Correlated Double Sampling for Mobile Applications C14: Phase-Locked Loops C14: To Bluetooth LE with PVT-Insensitive TUC Using Switched-Capacitor Double in 28nm CMOS C14: 1 16:00-16:25 A 0.5V 1.6mW 2.4GHz Fractional-N Al-Digital PLL for Bluetooth LE with PVT-Insensitive TUC Using Switched-Capacitor Double in 28nm CMOS C14:2 16:25-16:50 A Supply Noise Insensitive PLL with a Rail KAIST	C12-1 C12-1 KAIST C12-2 Univ. of Michigan C12-3 Semicondu ctor Energy Laboratory C12-4 National Tsing Hua Univ. C15-1 SK hynix C15-2 TSMC	12: SRAM & Emerging Memory 14:00-14:25 A 31.2pJ/disparity-pixel Stereo Matching Processor with Stereo SRAM for Mobile UI Application 14:26-14:50 A 0.3V VDDmin 4+2T SRAM for Searching and In-Memory Computing Using 55nm DDC Technology 14:50-15:15 A 140 MHz 1 Mbit 2T IC Gain-Cell Memory with 60-m Indum-Gailum-Zinc Oxide Transistor Embedded Into 65- mn CMOS Logic Process Technology 15:15-15:40 Embedded 2Mb ReRAM Macro with 2.6n Read Access Imme Using Dynamic-Trip-Point/match Sampling Current-Mode Sense Amplifer for ICE Applications Memory Interface and Flash Memory 16:00-16:25 A Floating Tap Termination Scheme with Inverted DBI AC and Floating Tap Forcing Technique of High-Speed Low-Power Signaling 16:25-16:50 A Resistor-Free 4.266 Gbps LPDDR4 I/O	C13: Bio C13-1 Univ. of Michigan C13-2 imec/Holst Centre C13-3 Univ. of Washington C13-4 imec/Holst Centre C16-1 KAIST C16-2 Seoul National	signal Recording / Monitoring Circuits 14:00-14:25 3.37 µW/Ch Modular Scalable Neural Recording System with Embedded Lossless Compression for Dynamic Power Reduction 14:25-14:50 A 36µW Reconfigurable Analog Front-End IC for Multimodal Vital Signs Monitoring 14:50-15:15 A Scalable, Highly-Multiplexed Delta-Encoded Digital Feedback ECoG Recording Amplifier with Common and Differential-Mode Artfact Suppression 15:15-15:40 A Bio-Impedance Readout IC with Frequency Sweeping from 1k-to-1MHz for Electrical Impedance Tomography 16: Dower Management Circuit 16:00-16:25 A 142:4% Power Edirection Improvement Energy Havesling Circuit with Smuttaneous Energy Eduction from a Plezofectric Transducer and A Thermoelectric Generator 16:251-6:50 A 2001-0:140mW Input Power Range, 94% Peak Efficiency Energy-Harvesting Battary Charger with	T9-1 IBM Research T9-2 IBM Research T9-3 The Univ. of Tokyo T9-4 IBM Research T11-1 GLOBALFC UNDRIES T11-2 Samsung	T9: 5 14:00-14:25 High Performance and Record Subthreshold Ge-Content Channels Formed by 3D Conder 14:25-14:50 SIGE FinFET for Practical Logic Libraries by 14:50-15:15 High Performance 4.5-nm-Thick Compressiv Condensation with Optimized Temperature 0 15:15-15:40 Understanding the Interfacial Layer Formatic Layer Hole Mobility T11: CM 16:00-16:25 14nm FinFET Technology for Analog and RF 16:25-16:50 High Performance 14nm FinFET Technology	iGe/Ge FET 1 Swing Demonstration in Scaled RMG SiGe FinFETs with High- isation and a Novel Gate Stack Process Mitigating Local Layout Effect ely-Strained Ge-On-Insulator pMOSFETs Fabricated by Ge control n on Strained Si _{1-x} Ge _x Channels and Their Correlation to Inversion IOS Integration I Cos Integration I Cos Power Mobile RF Application	T10-1 TSMC T10-2 KU Leuver T10-3 CEA-LETI T10-4 Peking Univ. T12-1 National Nano Device Laboratorise T12-2 Univ. of Notre	T10: Reliability 14:00-14:25 On-Die 16nm Metal Critical Peak Current Test Methodology with 100ps Pulse Width 14:25-14:50 A Fully-Integrated Method for RTN Parameter Extraction 14:50-15:15 New Insight on the Geometry Dependence of BT1 in 3D Technologies Based on Experiments and Modeling 15:15-15:40 Unified Self-Heating Effect Model for Advanced Digital and Analog Technology and Thermal- Aware Lifetime Prediction Methodology T12: Ferroelectric 16:00-16:25 Nano-Scaled Ge FinFETs with Low Temperature Ferroelectric HitZO, on Specific Interfacial Layers Exhibiting 65% S.S. Reduction and Improved Icsu 16:25-16:50 Impact of Total and Partial Dipole Switching on the Switching Slope of Gate-Last Negavic Capacitance FETs
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A 6Gb/s Rotatable Non-Contact Connector Bridge IC JFS2-3 14:50-16:15 TSMC High Density 3D Fanout Package for Heterogeneous Integration JFS2-4 15:15-15:40 XAIST System Using Multiple Digital Correlated Double Sampling for Mobile Applications C14: Phase-Locked Loops C14: Phase-Locked Loops C14: 1 16:00-16:25 A 0.5V 1.6mW 2:4GHz Fractional-N All-Digital PLL for Plateoth Lie With PVT-Insensitive DLC Using Switched-Capacitor Double in 28nm CMOS C14: 2 16:25-16:50 A Supply Noise Insensitive PLL with a Rail KAIST To-Rail Swing Ring Oscillator and a Wideband Noise Suppression and Robust Frequency Acquisition in 16nm FinFET C14: 1 16:30-17:15 XIIInx Based PLL with In-Band Noise Suppression and Robust Frequency Acquisition in 16nm FinFET C14: 17:15-17:40 Univ. of Computational Locking: Accelerating Locking: Accelerating Locking: Cacelerating Locking: Cacelerating Locking: Cacelerating Locking: Accelerat	C12-1 C12-1 C12-1 C12-2 C12-2 Univ. of Michigan C12-3 Semicondu ctor Energy Laboratory C12-4 National National National C15-1 C15-1 SK hynix C15-2 C15-3 Samsung Electronics C15-4 Univ. of C15-5	12: SRAM & Emerging Memory 14:00-14:25 A 31.2pJ/disparity pixel Stereo Matching Processor with Stereo SRAM for Mobile UI Application 14:25-14:50 A 0.3V VDDmin 4+2T SRAM for Searching and In-Memory Computing Using 55nm DDC Technology 14:50-15:15 A 140 MHz 1 Mit 2TI Cain-Cell Memory with 60-m Indum-Gallinz-Cell Memory with 60-m fuldms-Gallinz-Cell Memory With fixed-Data Cell Cell Cell Cell Memory With fixed-Cell Cell Cell Cell Cell Cell Memory With fixed-Cell Cell Memory Multi-Chip Package Employing F-Chip for Low Power and High Performance Storage Applications 17.15-17:40 An Ultra-Wide Program, 122pJ/Bit Flash Memory Using Charge Recycling 17.40-18:05	C13: Bio C13-1 Univ. of Michigan C13-2 imec/Holst Centre C13-3 Univ. of Washington C13-4 imec/Holst Centre C C16-1 KAIST C16-2 Seoul National Univ. C16-3 Korea Univ. C16-4 Northwestern Univ. C16-5	signal Recording / Monitoring Circuits 14:00-14:25 3:37 µW/Ch Modular Scalable Neural Recording System with Embedded Lossless Compression for Dynamic Power Reduction 14:25-14:50 A 36µW Reconfigurable Analog Front-End IC for Multimodal Vital Signs Monitoring 14:50-15:15 A Scalable, Highly-Multiplexed Delta-Encoded Digital Feedback EcoG Recording Amplifier with Common and Differential-Mode Artifact Suppression 15:15-15:40 A Bio-Impedance Readout IC with Frequency Sweeping from 1k-to-1MHz for Electrical Impedance Tomography 16:29 New Editaction Improvement Energy Havesling Crout with Simultaneous Energy Extraction form a Plezodetic Transducer and A Thermoelectric Cerenator 16:25-16:50 A 220tW-to-140mW Input Power Range, 94% Peak Effective Serge-Harvesting Battery Charger with Effective Serge-Harvesting Battery Charger Mattery A Serger Se	T9-1 IBM Research T9-2 IBM Research T9-3 The Univ. of Tokyo T9-4 IBM Research IBM Research T11-1 GLOBALFC UNDRIES T11-2 Samsung Electronics T11-3 Samsung Electronics T11-4 UNIST T11-5	T9: 5 14:00-14:25 High Performance and Record Subthreshold Ge-Content Channels Formed by 3D Conder 14:25-14:50 SiGe FinFET for Practical Logic Libraries by 14:50-15:15 High Performance 4.5-nm-Thick Compressiv Condensation with Optimized Temperature C 15:15-15:40 Understanding the Interfacial Layer Formatic Layer Hole Mobility T11: CM 16:00-16:25 14nm FinFET Technology for Analog and RF 16:25-16:50 High Performance 14nm FinFET Technology 16:50-17:15 10nm 2 nd Generation BEOL Technology with 17:15-17:40 Trantenna: Monolithic Transistor-Antenna De 17:40-18:05 (Late News)	iGe/Ge FET 1 Swing Demonstration in Scaled RMG SiGe FinFETs with High- isation and a Novel Gate Stack Process Mitigating Local Layout Effect ely-Strained Ge-On-Insulator pMOSFETs Fabricated by Ge Control n on Strained Si _{1-a} Ge _x Channels and Their Correlation to Inversion IOS Integration 1 * Applications • for Low Power Mobile RF Application Optimized Illumination and LELELELE wice for Real-Time THz Imaging System	T10-1 TSMC T10-2 KU Leuver T10-3 CEA-LETI T10-4 Peking Univ. T12-1 National Vano Device Laboratories T12-2 Univ. of Notre Dame T12-3 The Univ. of Tokyo T12-4 KU Leuver	T10: Reliability 14:00-14:25 On-Die 16nm Metal Critical Peak Current Test Methodology with 100ps Pulse Width 14:25-14:50 A Fully-Integrated Method for RTN Parameter Extraction 14:50-15:15 New Insight on the Geometry Dependence of BTi in 3D Technology and Dependence of BTi in 3D Technology and Thermal- Aware Lifetime Prediction Methodology 12:5 Ferroelectric 16:00-16:25 Nano-Scaled Ge FinFETs with Low Temperature Ferroelectric HEZO, on Specific Interfacial Layers Exhibing 5% S.S. Reduction and Improved IoN 16:25-16:50 Impact of Tatal and Partial Dipole Switching on the Switching Stope of Gate-Laxt Negative Capacitance FETs with Feroelectric HeHQ: Qapacitor for Normally- Off and Ultralow Power IoT Application 17:15-17:40 First Demonstration of Vertically Stacked Perroelectric Al Doped HfO2 Devices for NAND Applications
12:35-14:00 14:00-15:40 16:00-18:05	JFS2: Advanced Assembly JFS2-1 14:00-14:25 A Digitally Controlled Fully Integrated Voltage Regulator with 3D-TSV Based On-Die Sciend Inductor with Backside Planar Magnetic Core in 14rm Tri-Gate CMOS JFS2-2 14:25-14:50 A 6Gb/s Rotatable Non-Contact Connector Keio Univ. A 6Gb/s Rotatable Non-Contact Connector Bridge IC JFS2-3 14:50-15:15 TSMC High Density 3D Fanout Package for Heterogeneous Integration JFS2-4 15:15:15:40 KAIST System Using Multiple Digital Correlated Double Sampling for Mobie Applications C14-1 16:00-16:25 A 0.5V 1 SmW 2-4GHz Fractional-N Al-Digital PLL for Bulecoth LE with PVT-Insensitive DTC Using Switched-Capacitor Doubler in 28nm CMOS C14-2 16:25-16:50 A Supply Noise Insensitive PLL with a Rail KAIST To-Rail Swing Ring Oscillator and a Wideband Noise Suppression Loop C14-3 16:50-17:15 XIIInx Bade PLL with In-Ban Noise Suppression and Robust Frequency Acquisition in 16nm FinFET C14-4 17:15-17:40 Univ. of Computational Locking: Accelerating Lock Washington Times in All-Digital PLLs C14-5 17:40-18:05 A -242:48 FOM and -71-48c Reference Spur Ring Vol Berged Weight Put Ringeren	C12-1 C12-1 KAIST C12-2 Univ. of Michigan C12-3 Semicondu ctor Energy Laboratory C12-4 National Univ. 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T12-1 National Nano Device Laboratories T12-2 Univ. of Notre Dame T12-3 The Univ. of Tokyo T12-4 KU Leuver	T10: Reliability 14:00-14:25 On-Die 16nm Metal Critical Peak Current Test Methodology with 100ps Pulse Width 14:25-14:50 A Fully-Integrated Method for RTN Parameter Extraction 14:50-15:15 New Insight on the Geometry Dependence of BTI in 3D Technologies Based on Experiments and Modeling 15:15-15:40 Unified Self-Heating Effect Model for Advanced Digital and Analog Technology and Thermal- Aware Lifetime Prediction Methodology T12: Ferroselectric 16:00-16:25 Nano-Scaled Ge FinFETs with Low Temperature Ferroelectric Harbium Zirconium Oxide Gate Stack this Feroelectric Harbium Zirconium Oxide as task this Feroelectric Harbium Zirconium Oxide Stack this First Demonstration of Vertically Stacked Ferroelectric Al Doped HfO ₂ Devices for NAND Applications
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A 6Gb/s Rotatable Non-Contact Connector Bridge IC JFS2-3 14:50-15:15 TSMC High Density 3D Fanout Package for Heterogeneous Integration JFS2-4 15:15:15:40 KAIST System Using Multipe Digital Correlated Double Sampling for Moble Applications C14:1 16:00-16:25 C14:2 16:20-16:50 KAIST System Using Multipe Digital Correlated Double Sampling for Moble Applications C14:1 16:00-16:25 A 0.5V 1.6mW 2.4GH2 Fractional-N AI-Digital PLL for the Blacoton Lie with PVT-Insensitive TDC Using Switched-Capacitor Doubler in 28nm CMOS C14-2 16:25-16:50 A Suppl Noise Insensitive PLL with a Rail KAIST To-Rail Swing Ring Oscillator and a Wildeband Noise Suppression Loop C14-3 16:50-17:15 Xilinx A 164fs _{im} 9-to-18:05 Xilinx A 164fs _{im} 9-to-18:05 Xilinx A 164fs _{im}	C12-1 C12-1 C12-2 C12-2 Univ. of Michigan C12-3 Semicondu tor Energy Laboratory C12-4 National Tsing Hua Univ. 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C16-3 Korea Univ. C16-4 Northwestern Univ. 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T12-1 National Nano Device Laboratories T12-2 Univ. of Notre Dame T12-3 The Univ. of Tokyo T12-4 KU Leuver	T10: Reliability 14:00-14:25 On-Die 16nm Metal Critical Peak Current Test Methodology with 100ps Pulse Width 14:25-14:50 A Fully-Integrated Method for RTN Parameter Extraction 14:50-15:15 New Insight on the Geometry Dependence of BTI in 3D Technologies Based on Experiments and Modeling 15:15-15:40 Unified Self-Heating Effect Model for Advanced Digital and Analog Technology and Thermal- Aware Lifetime Prediction Methodology T12: Ferroelectric 16:00-16:25 Nano-Scaled Ge FirFETs with Low Temperature Ferroelectric Harty.or on Specific Interfacial Layers Exhibiting 65% S.S. Reduction and Improved Iox 16:25-17:15 A Nonvolatile SRAM Integrated with Ferroelectric Harty.or Capacitor for Normally- Off and Ultralow Power IoT Application 17:15-17:40 First Demonstration of Vertically Stacked of Ferroelectric Al Doped HfO ₂ Devices for NAND Applications
12:35-14:00	JFS2: Advanced Assembly JFS2-1 14:00-14:25 A Digitally Controlled Fully Integrated Voltage Regulator with 3D-TSV Based non-be Sciend Inductor with Backside Planar Magnetic Care in 14m Tri-Gate CMOS JFS2-2 14:25-14:50 A 6Gb/s Rotatable Non-Contact Connector Keio Univ. A 6Gb/s Rotatable Non-Contact Connector With High-Speed/l ² C/CAN/SPI Interface Bridge IC JFS2-3 14:50-15:15 TSMC High Density 3D Fanout Package for Heterogeneous Integration JFS2-4 15:15:15-40 KAIST System Using Multiple Digital Correlated Double Sampling for Mobile Applications C14-1 16:00-16:25 C14-2 16:25-16:50 KAIST System Using Multiple Digital Correlated Double Sampling for Mobile Applications C14-1 16:00-16:25 X A 0.5V 1.8mW 2.4GHz Fractional-N AI-Digital PLL for Blautoab LE with PVT-Insensitive TDC Using Switched-Capacitor Doubler in 28nm CMOS C14-2 16:25-16:50 A Supply Noise Insensitive PLL with a Rail To-Rail Swing Ring Oscillator and a Wildeband Noise Suppression Loop C14-3 16:50-17:15 A 164fs _{mm} 9-to-18:GHz Sampling Phase Detector Based PLL with In-Band Noise Suppression and Robust Frequency Acquisition in 16m FinFET C14-4	C12-1 C12-1 C12-2 Univ. of Michigan C12-3 Semicondu clor Energy Laboratory C12-4 National Tsing Hua Laboratory C12-4 National Tsing Hua Laboratory C12-1 C15-1 C15-1 C15-1 C15-2 C15-2 C15-3 Samsung Electronice C15-3 Samsung Electronice C15-5 TSMC	12: SRAM & Emerging Memory 14:00-14:25 A 31.2pJ/disparity pixel Stereo Matching Processor with Stereo SRAM for Mobile UI Application 14:25-14:50 A 0.3V VDDmin 4+2T SRAM for Searching and In-Memory Computing Using 55nm DDC Technology 14:50-15:15 A 140 MH-1 Mill 2TI Gain-Cell Memory with 60-m Indum-Gallwarz Code Transfer Embedded Into 65- mm CMOS Logic Process Technology 15:15-15:40 Embedded 2Mb ReRAM Macro with 2.6ns Read Access Time Using Dynamic-Trip-Point-Mismatch Sampling Current-Mode Series Amplifies for IG-Applications 40m ory Interface and Flash Memory 16:00-16:25 A Floating Tap Termination Scheme with Inverted DBL AC and Floating Tap Forcing Technology 16:50-17:15 A 1.2V 1.33Gb/s/pin 8Tb NAND Flash Memory Mulli- Chip Package Employing F-Chip for Low Power and High Performance Storage Applications 17:15-17:40 An Ultra-Wide Program, 122pJ/Bit Flash Memory Using Charge Recycling 17:40-18:05 A 40m Spil Gate Embedded Flash Macro with Flexible 2- in-1 Architecture, Code Memory with 140UHz Read Speed and Data Memory with 140U/Lick Read Speed and Data Memory with 140U/Lick Read Speed A dom Spil Gate Embedded Flash Macro with Flexible 2- in-1-Architecture, Code Memory with 140U/Lick Read Speed and Data Memory with 140U/Lick Read Speed	C13: Bio C13-1 Univ. of Michigan C13-2 imec/Holst Centre C13-3 Univ. of Washington C13-4 Univ. of Washington C13-4 Centre C13-4 Centre C13-4 Centre C16-1 KAIST C16-2 Seoul National Univ. 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T12-1 National Nano Device Laboratories T12-2 Univ. of Notre Dame T12-3 The Univ. of Tokyo T12-4 KU Leuver	T10: Reliability 14:00-14:25 On-Die 16nm Metal Critical Peak Current Test Methodology with 100ps Pulse Width 14:25-14:50 A Fully-Integrated Method for RTN Parameter Extraction 14:50-15:15 New Insight on the Geometry Dependence of BT1 in 3D Technologies Based on Experiments and Modeling 15:15-15:40 Unified Self-Heating Effect Model for Advanced Digital and Analog Technology and Thermai- Aware Lifetime Prediction Methodology T12: Ferroelectric 16:00-16:25 Nano-Scaled Ge FinFETs with Low Temperature Ferroelectric Hardia Area Negative Capacitance FETs with Ferroelectric Hafum Zirconum Oxide are Stack 16:50-17:15 A Nonvolatile SRAM Integrated with Ferroelectric H102 Capacitor for Normally- Off and Ultralow Power IoT Application 17:15-17:40 First Demonstration of Vertically Stacked n Ferroelectric Al Doped HT02 Devices for NAND Applications

2017 Symposia on VLSI Technology and Circuits June 8th (Thursday)

 Hand Biological Control C			Suzaku III		Suzaku II		Suzaku I		Shunju III	Shunju II		Shunju I
No. Control Number 2000 Contro Number 2000 Cont	8:00-17:00			Registration (Technology and Circuits)								
No. No. <td></td> <td></td> <td>C17: Video Processing</td> <td></td> <td>C18: SAR ADCs</td> <td></td> <td>C19: Image Sensors</td> <td></td> <td>JFS3: Ultra Lov</td> <td>w Power for IoT</td> <td>T13: 0</td> <td>Quantum Neuromorphic Computing</td>			C17: Video Processing		C18: SAR ADCs		C19: Image Sensors		JFS3: Ultra Lov	w Power for IoT	T13: 0	Quantum Neuromorphic Computing
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Number Number<			System Architecture with Single Chip 8K		A 2.4-mW 25-MHz BW 300-MS/s Passive	Sony	A 4.1Mpix 280fps Stacked CMOS Image					Towards Quantum Computing in Si MOS Technology:
No. 10 No. 10<		Socionext	HEVC Decoder for 8K Advanced BS Receiver System	Medialek	Noise Shaping SAR ADC with Noise	Semiconduct or Solutions	Sensor with Array-Parallel ADC Architecture for Region Control	DENSO	Computing Platform for Automotive Electron	nics of Automated Driving Generation	CEA-LE II	Single-Shot Readout of Spin States in a FDSOI Split-Gate Device with Built-In Charge Detector
State State <th< td=""><td rowspan="2"></td><td>C17-2</td><td>8:55-9:20</td><td>C18-2</td><td>8:55-9:20</td><td>C19-2</td><td>8:55-9:20</td><td>JFS3-2</td><td>8:55-9:20 (Invited)</td><td></td><td>T13-2</td><td>8:55-9:20</td></th<>		C17-2	8:55-9:20	C18-2	8:55-9:20	C19-2	8:55-9:20	JFS3-2	8:55-9:20 (Invited)		T13-2	8:55-9:20
Hama Non- series		Univ of	A 127mW 1.63TOPS Sparse Spatio-Temporal	The Univ.	A 12h ENOD 172dD EaM 2 nd Order NG		A 256 Energy Bin Spectrum X-Ray Photon-Counting Image				Sandia	Achieving Ideal Accuracies in Analog
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$ \frac{1}{10} $	0:30-10:10	C17-3	Notion Tracking in videos	Austin C18-3	0:20-0:45	C10-3	9:20.9:45	IES3-3	9:20-9:45		T13-3	3 Carry 9:20-9:45
Image: Note:		017-5	A Single-Chip 2048×1080 Resolution 32fps	National	3.20-3.40	013-5	A 0.61 E- Noise Global Shutter CMOS	United	5.20-5.45	<u></u>	115-5	3.20-3.40
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No. No. <td></td> <td>C20-1</td> <td>10:30-10:55</td> <td>C21-1</td> <td>10:30-10:55</td> <td></td> <td></td> <td>JFS4-1</td> <td>10:30-10:55 (Invited)</td> <td></td> <td>114-1</td> <td>10:30-10:55</td>		C20-1	10:30-10:55	C21-1	10:30-10:55			JFS4-1	10:30-10:55 (Invited)		114-1	10:30-10:55
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		Michigan	Cryptographic Cortex-M0 Processor for IoT	Zurich	Mode-Regulation DAC in 14nm CMOS FinFET			Research	·····		-	Enhancement in UTB GeOInMOSFETs
Name Addition Addition <th< td=""><td></td><td>C20-2</td><td>10:55-11:20</td><td>C21-2</td><td>10:55-11:20</td><td></td><td></td><td>JFS4-2</td><td>10:55-11:20 (Invited)</td><td></td><td>T14-2</td><td>10:55-11:20</td></th<>		C20-2	10:55-11:20	C21-2	10:55-11:20			JFS4-2	10:55-11:20 (Invited)		T14-2	10:55-11:20
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No. No. Subject Algebrain Control Contro Control Control		C20-4	11:45-12:10	C21-4	11:45-12:10			JFS4-4	11:45-12:10		T14-4	11:45-12:10
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Dist Dist <thdis< th=""> Dist Dist D</thdis<>		Michigan	Response PUF Using 28nm SRAM 6T Bit	Devices	Calibration in 55nm CMOS			Univ.	Featuring Nonvolatile Logics and Processin	ng-In-Memory	Univ. of	Achieving Lowest S of 79 mV/decade and Record High G in of 807 uS/um for GeSn P-FETs
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14/10/14/20 14/10/14/20 10/10/14/20		C22.	(CES) Advanced Sensing Systems	C23: High-	Speed and Power Efficient Wireless Transceivers		as a Part of Body		T15: Memory 2	2 Elash MRAM		T16: Process
Num Solution Solution Column		C22-1	14:00-14:25 (Invited)	C23-1	14:00-14:25			T15-1	14:00-14:25		T16-1	14:00-14:25
Number Process Process <th< td=""><td></td><td>Sony</td><td>320x240 Back-Illuminated 10µm CAPD</td><td>Tokyo</td><td>A 100mW 3.0 Gb/s Spectrum Efficient 60</td><td></td><td></td><td>Samsung</td><td>High-Speed and Logic-Compatible Split-Ga</td><td>te Embedded Elash on 28-nm I ow-Power HKMG I ogic</td><td></td><td>Dual Beam Laser Annealing for Contact</td></th<>		Sony	320x240 Back-Illuminated 10µm CAPD	Tokyo	A 100mW 3.0 Gb/s Spectrum Efficient 60			Samsung	High-Speed and Logic-Compatible Split-Ga	te Embedded Elash on 28-nm I ow-Power HKMG I ogic		Dual Beam Laser Annealing for Contact
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14:00:15:00 223.3 14:50:15:15 16:30:16:10 16:30:16:15:15 16:30:16:15:15:16:00 16:30:16:15:15:16:10:10 16:30:16:15:15:16:10:10 16:30:16:15:15:16:10:10 16:30:16:15:15:16:10 16:30:16:15:15:16:10 16:30:16:15:15:16:10 16:30:16:15:15:16:10 16:30:16:15:15:16:10 16:30:16:15:15:15:16:10 16:30:16:15:15:15:16:10 16:30:16:15:15:15:16:10 16:30:16:15:15:15:15:16:10 16:30:16:15:15:15:15:15:15:15:15:15:15:15:15:15:			14:25-14:50 (Invited) An Imager Using 2-D Single-Photon	C23-2	14:25-14:50 A 230-260GHz Wideband Amplifier in 65nm			T15-2 Seoul	14:25-14:50 First Demonstration of Diode-Type 3-D NAN	ND Flash Memory String Having Super-Steen Switching	Research	VLSI Integrated Circuit Variability 14:25-14:50 Sub-10 ⁻⁹ Ω.cm ² Contact Resistivity on p-
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C224151:51:5:40C234151:51:5:40T164151:51:5:40T164151:51:5:40 $V62$ 0.223:4:1:0:1:0:0:0:0:0:0:0:0:0:0:0:0:0:0:0:0	14:00-15:40	DENSO C22-3 Univ. of Edinburgh	14:25-14:50 (Invited) An Imager Using 2-D Single-Photon Avalanche Diode Array in 0.18-µm CMOS for Automotive LIDAR Application 14:50-15:15 A 16.5 Giga Events/s 1024 × 8 SPAD Line Sensor with Per-Pixel Zoomable 50ps-	C23-2 KAIST C23-3 Univ. of California,	14:25-14:50 A 230-260GHz Wideband Amplifier in 65nm CMOS Based on Dual-Peak G _{max} -Core 14:50-15:15 A 65nm CMOS I/Q RF Power DAC with 24 - 420B 3 rd Harmonic Cancellation and up to			T15-2 Seoul National Univ. T15-3 Chuo Univ.	14:25-14:50 First Demonstration of Diode-Type 3-D NAN Slope 14:50-15:15 Flash Reliability Boost Huffman Coding (FR Plasting Modulation to Ephance Data-Re-	ND Flash Memory String Having Super-Steep Switching RBH): Co-Optimization of Data Compression and V _{TH} elemention Time by Over 2000x	TI6-2 imec IBM Research IBM Research	VLSI Integrated Circuit Variability 14:25-14:50 Sub-10 ⁹ Ω.cm ² Contact Resistivity on p- SiGe Achieved by Ga Doping and Nanosecond Laser Activation 14:50-15:15 Highly-Selective Superconformal CVD Ti Silicid Process Enabling Area-Enhanced Contacts for
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T15-4 GLOBALFO UNDRIES T17-1 GLOBALFO UNDRIES</td> <td>14:25-14:50 First Demonstration of Diode-Type 3-D NAN Slope 14:50-15:15 Flash Reliability Boost Huffman Coding (FR Distribution Modulation to Enhance Data-Reliability Boost Huffman Coding (FR Distribution Modulation to Enhance Data-Reliability Boost Huffman Coding (FR Distribution Modulation to Enhance Data-Reliability Boost Huffman Coding (FR 15:15-15:40 CMOS-Embedded STT-MRAM Arrays in 2x T17: CMOS I 16:00-16:25 Low-Variation SRAM Bitcells in 22nm FDSC</td> <td>ND Flash Memory String Having Super-Steep Switching RBH): Co-Optimization of Data Compression and V_{TH} etention Time by Over 2900x a nm Nodes for GP-MCU Applications Integration II DI Technology</td> <td>IBM Research T16-2 imec T16-3 IBM Research T16-4 National Univ. of Singapore</td> <td>VLSI Integrated Circuit Variability 14:25-14:50 Sub-10³ 0.cm² Contact Resistivity on p-SiGe Achieved by Ga Doping and Nanosecond Laser Activation 14:50-15.15 Highly-Selective Superconformal CVD Ti Silicid Process Enabling Area-Enhanced Contacts for Next-Generation CMOS Architectures 15:15-15:40 Record Low Specific Contact Resistivity (1.2×10⁶ q.cm³) for P-Type Semiconductors: Incorporation of Sr into Ge and <i>In-Situ</i> Ga Doping</td>	14:00-15:40	DENSO C22-3 Univ. of Edinburgh C22-4 Univ. of Michigan C24-1 KAIST	14:25-14:50 (Invited) An Imager Using 2-D Single-Photon Avalanche Diode Array in 0.18- µm CMOS for Automotive LIDAR Application 14:50-15:15 A 16:5 Giga Events/s 1024 × 8 SPAD Line Sensor with Per-Pixel Zoomable 50ps- 6.4ns/bin Histogramming TDC 15:15-15:40 A 272.49 µJ/kel CMOS Image Sensor with Embedded Object Detection and Bio-Inspired 2D Optic Flow Generation for Nano-Air-Vehicle Navigation C23: Physical Sensors 16:00-16:25 A 10:1*66-Channel, 183 uWelectode, 0.73 mm ⁷ Jensor	KAIST C23-2 KAIST C23-3 Univ. of California, Berkeley C23-4 Renesas Electronics C25-1 IBM T.J. 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T15-4 GLOBALFO UNDRIES T17-1 GLOBALFO UNDRIES	14:25-14:50 First Demonstration of Diode-Type 3-D NAN Slope 14:50-15:15 Flash Reliability Boost Huffman Coding (FR Distribution Modulation to Enhance Data-Reliability Boost Huffman Coding (FR Distribution Modulation to Enhance Data-Reliability Boost Huffman Coding (FR Distribution Modulation to Enhance Data-Reliability Boost Huffman Coding (FR 15:15-15:40 CMOS-Embedded STT-MRAM Arrays in 2x T17: CMOS I 16:00-16:25 Low-Variation SRAM Bitcells in 22nm FDSC	ND Flash Memory String Having Super-Steep Switching RBH): Co-Optimization of Data Compression and V _{TH} etention Time by Over 2900x a nm Nodes for GP-MCU Applications Integration II DI Technology	IBM Research T16-2 imec T16-3 IBM Research T16-4 National Univ. of Singapore	VLSI Integrated Circuit Variability 14:25-14:50 Sub-10 ³ 0.cm ² Contact Resistivity on p-SiGe Achieved by Ga Doping and Nanosecond Laser Activation 14:50-15.15 Highly-Selective Superconformal CVD Ti Silicid Process Enabling Area-Enhanced Contacts for Next-Generation CMOS Architectures 15:15-15:40 Record Low Specific Contact Resistivity (1.2×10 ⁶ q.cm ³) for P-Type Semiconductors: Incorporation of Sr into Ge and <i>In-Situ</i> Ga Doping
System for Aeronautic Applications Research CMOS Fin FET SRPG/DVFS and Temperature Tracking Clocks 16:00-18:05 C24-3 16:50-17:15 C26-3 16:50-17:15 C26-3 16:50-17:15 T17-3 16:50-17:15 16:00-18:05 A 6x5x4mm ³ General Purpose Audio Sensor Node with a 4.7µW Audio Processing IC NTT A 2.25-mW(Gb/s 80-Gb/s-PAM4 Linear Driver with a Single Supply Using Stacked California, Driver with a Single Supply Using Stacked California, Processing IC C26-4 17:15-17:40 C26-4 17:15-17:40 C26-4 17:15-17:40 C26-4 17:15-17:40 T17-4 17:15-17:40 Univ. of Michigan A 4.7µW Switched-Bias MEMS Microphore Preamplifier for Ultra-Low-Power Voice Xilinx A 2.66/b/s 8.1-mW Receiver with Linear Sampling Phase Detector for Data and Edge Equalization Tsinghua Speed and 11+ Higher Energy Efficiency Using Fast Pereir Univ. Tr:40 17:40 17:40 17:40 16:50-17:15 Univ. of Michigan A 4.7µW Switched-Bias MEMS Microphore Preamplifier for Ultra-Low-Power Voice Xilinx A 28-Gb/s 8.1-mW Receiver with Linear Sampling Phase Detector for Data and Univ. Tsinghua Speed and 11+ Higher Energy Efficiency Using Fast Power Univ. GLOBALFO NoDetector and Nonvolable Eador Controler GLOBALFO Univ. Influence of Stress Induced CT Local Layout Effect (LLE) on 14nm FinFET GLOBALFO UNDRIES GLOBALFO U	14:00-15:40	DENSO C22-3 Univ. of Edinburgh C22-4 Univ. of Michigan C24-1 KAIST C24-2	14:25-14:50 (Invited) An Imager Using 2-D Single-Photon Avalanche Diode Array in 0.18- µm CMOS for Automotive LIDAR Application 14:50-15:15 A 16:5 Giga Events/s 1024 × 8 SPAD Line Sensor with Per-Pixel Zoomable 50ps- 6.4ns/bin Histogramming TDC 15:15-15:40 A 272 40 pJ/kel CMOS Image Sensor with Embedded Object Detection and Bio-Inspired 2D Optic Flow Generation for Nano-Air-Vehicle Navigation C22: Physical Sensors 16:00-16:25 A 10:1*66-Channel, 183 UWelectode, 0.73 mm ⁷ /sensor High SNR 3D Hover Sensor Based on Enhanced Signal Rehing and Fine Error Calibrating Techniques 16:25-16:50	C23-2 KAIST C23-3 Univ. of California, Berkeley C23-4 Renesas Electronics C25-1 IBM T.J. Watson Research Center C25-2	14:25-14:50 A 230-260GHz Wideband Amplifier in 65nm CMOS Based on Dual-Peak G _{max} -Core 14:50-15:15 A 65nm CMOS I/Q RF Power DAC with 24 - 42dB 3 rd Harmonic Cancellation and up to 18:dB Mixed-Signal Filtering 15:15-15:40 A 43%-Efficiency 20dBm Sub-GHz Transmitter Employing Rise-Edge-Synchronized Harmonic Calibration with 33.3% Duty Cycle 5: High-Speed Wireline Circuits 16:00-16:25 A 32Gb/s, 4.7p.J/bit Optical Link with – 11.7dBm Sensitivity in 14nm FinFET CMOS 16:25-16:50 A 50 Gb/s 1.9 Di/bit NPZ Ontical Encenting	C26-1 National Taiwan Univ. C26-2	C26: Processors and SoC 16:00-16:25 A 501 mW 7.61 Gb/s Integrated Message- Passing Detector and Decoder for Polar- Coded Massive MIMO Systems 16:25-16:50	T15-2 Seoul National Univ. T15-3 Chuo Univ. T15-4 GLOBALFO UNDRIES T17-1 GLOBALFO UNDRIES T17-2	14:25-14:50 14:25-14:50 First Demonstration of Diode-Type 3-D NAN Slope 14:50-15:15 Flash Reliability Boost Huffman Coding (FR Distribution Modulation to Enhance Data-Re 15:15-15:40 CMOS-Embedded STT-MRAM Arrays in 2x T17: CMOS I 16:00-16:25 Low-Variation SRAM Bitcells in 22nm FDSC 16:25-16:50	ND Flash Memory String Having Super-Steep Switching RBH): Co-Optimization of Data Compression and V _{TH} etention Time by Over 2900x a nm Nodes for GP-MCU Applications Integration II DI Technology	IBM Research T16-2 imec T16-3 IBM Research T16-4 National Univ. of Singapore	VLSI Integrated Circuit Variability 14:25-14:50 Sub-10 ³ 0.cm ² Contact Resistivity on p-SiGe Achieved by Ga Doping and Nanosecond Laser Activation 14:50-15:15 Highly-Selective Superconformal CVD Ti Silicid Process Enabling Area-Enhanced Contacts for Next-Generation CMOS Architectures 15:15-15:40 Record Low Specific Contact Resistivity (1.2×10 ⁶ q.cm ³) for P-Type Semiconductors: Incorporation of Sr into Ge and <i>In-Situ</i> Ga Doping
16:50-17:15 C2F-3 16:50-17:15 C2F-3 16:50-17:15 C2F-3 16:50-17:15 10:wiv. of Nickigan A 6x5×4mm ³ General Purpose Audio Processing IC NTT Driver with a Single Supply Using Stacked California, Driver with a Single Supply Using Stacked California, Current-Mode Architecture in 65-nm CMOS Viv. of California, Driver with a Single Supply Using Stacked California, Driver with a Single Supply Using Stacked California, Current-Mode Architecture in 65-nm CMOS C26-4 17:15-17:40 C2F-1 Key Process Steps for High Performance and Reliable 3D Sequential Integration California, Decoder for Storage Applications C2F-1 17:15-17:40 C2F-1 C2F-1 Key Process Steps for High Performance and Reliable 3D Sequential Integration California, Decoder for Storage Applications C2F-1 17:15-17:40 C2F-1 T17:4 17:15-17:40 C2F-4 17:15-17:40 C26-4 17:15-17:40 C26-4 17:15-17:40 C2F-1 T17:4 17:15-17:40 Univ. of Nichigan A 4:7/W Switched-Bias MEMS Microphone Preamplifier for Ultra-Low-Power Voice Interfaces A 26:Gb/s 8:1-mW Receiver with Linear Sampling Phase Detector for Data and Edge Equalization Tion FERAMetased Parallel Recover Nonvolate Factor On Detection and Nonvolat	14:00-15:40	DENSO C22-3 Univ. of Edinburgh C22-4 Univ. of Michigan C24-1 KAIST C24-2 CEA-LETI	14:25-14:50 (Invited) An Imager Using 2-D Single-Photon Avalanche Diode Array in 0.18- µm CMOS for Automotive LIDAR Application 14:50-15:15 A 16.5 Giga Events/s 1024 × 8 SPAD Line Sensor with Per-Pixel Zoomable 50ps- 6.4ns/bin Histogramming TDC 15:15-15:40 A 272.49 µJpixel CMOS Image Sensor with Embedded Object Detection and Bio-Inspired 20 Optic Flow Generator for Nano-Air-Vehicle Navigation C24: Physical Sensors 16:00-16:25 A 10.1*56-Channel, 183 uWielectrode, 0.73 mm ⁷ /sensor High SNR 3D Hover Sensor Based on Enhanced Signal Enhing and Fine Error Calibrating Techniques 16:25-16:50 A Robust and Versatile, -40°C to +180°C, 8Sps	C23-2 KAIST C23-3 Univ. of California, Berkeley C23-4 Renesas Electronics C25-1 IBM T.J. Watson Research Center C25-2 IBM	14:25-14:50 A 230-260GHz Wideband Amplifier in 65nm CMOS Based on Dual-Peak G max-Core 14:50-15:15 A 65nm CMOS I/Q RF Power DAC with 24 - 42dB 3 rd Harmonic Cancellation and up to 18dB Mixed-Signal Filtering 15:15-15:40 A 43%-Efficiency 20dBm Sub-GHz Transmitter Employing Rise-Edge-Synchronized Harmonic Calibration with 33.3% Duty Cycle 5: High-Speed Wireline Circuits 16:00-16:25 A 32Gb/s, 4.7pJ/bit Optical Link with 11.7dBm Sensitivity in 14nm FinFET CMOS 16:25-16:50 A 60 Gb/s 1.9 PJ/bit NRZ Optical-Receiver with Low Latency Diotal CDR in 14nm	C26-1 National Taiwan Univ. C26-2 ARM	C26: Processors and SoC 16:00-16:25 A 501mW 7.61Gb/s Integrated Message- Passing Detector and Decoder for Polar- Coded Massive MIMO Systems 16:25-16:50 A 12:4pJ/cycle Sub-Threshold, 16pJ/cycle Near- Threshold ARK Cortex-Mot McU with Autonomous	T15-2 Seoul National Univ. T15-3 Chuo Univ. T15-4 GLOBALFO UNDRIES T17-1 GLOBALFO UNDRIES T17-2 CEA-LETI	14:25-14:50 14:25-14:50 First Demonstration of Diode-Type 3-D NAN Slope 14:50-15:15 Flash Reliability Boost Huffman Coding (FR Distribution Modulation to Enhance Data-Ro 15:15-15:40 CMOS-Embedded STT-MRAM Arrays in 2x 16:00-16:25 Low-Variation SRAM Bitcells in 22nm FDSC 16:25-16:50 Impact of Strain on Access Resistance in P	ND Flash Memory String Having Super-Steep Switching RBH): Co-Optimization of Data Compression and V _{TH} etention Time by Over 2900x www.sciencestor.com www.sciencestor.com Integration II DI Technology Ianar and Nanowire CMOS Devices	IBM Research T16-2 imec T16-3 IBM Research T16-4 National Univ. of Singapore	VLSI Integrated Circuit Variability 14:25-14:50 Sub-10 ³ Ω.cm ² Contact Resistivity on p- SiGe Achieved by Ga Doping and Nanosecond Laser Activation 14:50-15.15 Highly-Selective Superconformal CVD Ti Silicid Process Enabling Area-Enhanced Contacts for Next-Generation CMOS Architectures 15:15-15:40 Record Low Specific Contact Resistivity (1.2×10 ⁹ Q- cm ³) for P-Type Semiconductors: Incorporation of Sr into Ge and <i>In-Situ</i> Ga Doping
Univ. of Michigan A 0-03-willint General PulpOse Audio Sensor Node with a 4.7 µW Audio Processing IC NTT NTT Driver with a Single Supply Using Stacked Current-Mode Architecture in 65-nm CMOS A 2.267 Gbps, 93.7 pJ/b Non-Binary LDPC Decode for Storage Applications CEA-LET Key Process Steps for High Performance and Reliable 3D Sequential Integration C244 17:15-17:40 C25-4 17:15-17:40 C26-4 17:15-17:40 T17-4 17:15-17:40 Univ. of Michigan A 4.7 µW Switched-Bias MEMS Microphone Preamplifier for Ultra-Low-Power Voice Xilinx Sampling Phase Detector for Data and Edge Equalization Tsinghue Prover With 3 6:100 m FeRAM-Based Parallel Recovery Nonvolatile Radio Controller CloBALFO Niviv. Univ. of Preamplifier for Ultra-Low-Power Voice Xilinx Sampling Phase Detector for Data and Univ. Tsinghue Protection and Nonvolatile Radio Controller Tsin	14:00-15:40	DENSO C22-3 Univ. of Edinburgh C22-4 Univ. of Michigan C24-1 KAIST C24-2 CEA-LETI	14:25-14:50 (Invited) An Imager Using 2-D Single-Photon Avalanche Diode Array in 0.18-µm CMOS for Automotive LIDAR Application 14:50-15:15 A 16.5 Giga Events/s 1024 × 8 SPAD Line Sensor with Per-Pixel Zoomable 50ps- 6.4ns/bin Histogramming TDC 15:15-15:40 A 272-40 pJpixel CMOS Image Sensor with Embedded Object Detection and Bio-Inspired 2D Optic Flow Generator for Nano-Air-Vehicle Navigation C24: Physical Sensors 16:00-16:25 A 10.1*56-Channel, 183 uWelectrode, 0.73 mm ⁷ sensor High SNR 3D Hover Sensor Based on Enhanced Signal Refining and Fine Error Calibrating Techniques 16:25-16:50 A Robust and Versatile, -40°C to +180°C, 85ps to 1x5ps, Multi Power Source Wireless Sensor System for Aeronautic Applications	C23-2 KAIST C23-3 Univ. of California, Berkeley C23-4 Renesas Electronics C25-1 IBM T.J. Watson Research Center C25-2 IBM Research	14:25-14:50 A 230-260GHz Wideband Amplifier in 65nm CMOS Based on Dual-Peak G _{max} -Core 14:50-15:15 A 65nm CMOS I/Q RF Power DAC with 24 - 42dB 3 rd Harmonic Cancellation and up to 18dB Mixed-Signal Filtering 15:15-15:40 A 43%-Efficiency 20dBm Sub-GHz Transmitter Employing Rise-Edge-Synchronized Harmonic Calibration with 33.3% Duty Cycle 5: High-Speed Wireline Circuits 16:00-16:25 A 32Gb/s, 4.7pJ/bit Optical Link with – 11.7dBm Sensitivity in 14nm FinFET CMOS 16:25-16:50 A 60 Gb/s 1.9 Pj/bit NRZ Optical-Receiver with Low Latency Digital CDR in 14nm CMOS FinFET	C26-1 National Taiwan Univ. C26-2 ARM	C26: Processors and SoC 16:00-16:25 A 501mW 7.61Gb/s Integrated Message- Passing Detector and Decoder for Polar- Coded Massive MIMO Systems 16:25-16:50 A 12:4pJ/cyde Sub-Threshold, floJ/cyde Near- Threshold ARK Cortex-Mot With Autonomous SRPG/DVFS and Temperature Tracking Clocks	T15-2 Seoul National Univ. T15-3 Chuo Univ. T15-4 GLOBALFO UNDRIES T17-1 GLOBALFO UNDRIES T17-2 CEA-LETI	14:25-14:50 14:25-14:50 First Demonstration of Diode-Type 3-D NAN Slope 14:50-15:15 Flash Reliability Boost Huffman Coding (FR Distribution Modulation to Enhance Data-Ro 15:15-15:40 CMOS-Embedded STT-MRAM Arrays in 2x T17: CMOS I 16:00-16:25 Low-Variation SRAM Bitcells in 22nm FDSC 16:25-16:50 Impact of Strain on Access Resistance in PI	ND Flash Memory String Having Super-Steep Switching RBH): Co-Optimization of Data Compression and V _{TH} etention Time by Over 2900x Integration II OI Technology Ianar and Nanowire CMOS Devices	IBM Research T16-2 imec T16-3 IBM Research T16-4 National Univ. of Singapore	VLSI Integrated Circuit Variability 14:25-14:50 Sub-10 ³ Ω.cm ² Contact Resistivity on p- SiGe Achieved by Ga Doping and Nanosecond Laser Activation 14:50-15.15 Highly-Selective Superconformal CVD Ti Silicid Process Enabling Area-Enhanced Contacts for Next-Generation CMOS Architectures 15:15-15:40 Record Low Specific Contact Resistivity (1.2×10 ⁶ o- cm ³) for P-Type Semiconductors: Incorporation of Sr into Ge and In-Situ Ga Doping
Micrigan Processing IC Current-Mode Architecture in 65-nm CMOS Los Angeles Decoder for Storage Applications C24-4 17:15-17:40 C25-4 17:15-17:40 C26-4 17:15-17:40 T17-4 17:15-17:40 Univ. of Michigan A 26-Gb/s 8.1-mW Receiver with Interfaces A 26-Gb/s 8.1-mW Receiver with Sampling Phase Detector for Data and Edge Equalization Tsings have and there are prainter Receiver with Univ. Tsings have and the	14:00-15:40	DENSO C22-3 Univ. of Edinburgh C22-4 Univ. of Michigan C24-1 KAIST C24-2 CEA-LETI C24-3	14:25-14:50 (Invited) An Imager Using 2-D Single-Photon Avalanche Diode Array in 0.18-µm CMOS for Automotive LIDAR Application 14:50-15:15 A 16.5 Giga Events/s 1024 × 8 SPAD Line Sensor with Per-Pixel Zoomable 50ps- 6.4ns/bin Histogramming TDC 15:15-15:40 A 272.49 µJpixel CMOS Image Sensor with Embedded Object Detection and Bio-Inspired 2D Optic Flow Generator for Nano-Air-Vehicle Navigation C24: Physical Sensors 16:00-16:25 A 10.1*56-Channel, 183 uWelectrode, 0.73 mm ² /sensor High SNR 3D Hover Sensor Based on Enhanced Signal Refining and Flow Flow Source Wireless Sensor 16:25-16:50 A Robust and Versatile, -40°C to +180°C, 85ps to 1kSps, Multi Power Source Wireless Sensor System for Aeronautic Applications	C23-2 KAIST C23-3 Univ. of California, Berkeley C23-4 Renesas Electronics C25-1 IBM T.J. Walson Center C25-2 IBM Research C25-3	14:25-14:50 A 230-260GHz Wideband Amplifier in 65nm CMOS Based on Dual-Peak G _{max} -Core 14:50-15:15 A 65nm CMOS I/Q RF Power DAC with 24 - 42dB 3 rd Harmonic Cancellation and up to 18dB Mixed-Signal Filtering 15:15-15:40 A 43%-Efficiency 20dBm Sub-GHz Transmitter Employing Rise-Edge-Synchronized Harmonic Calibration with 33:3% Duty Cycle 5: High-Speed Wireline Circuits 16:00-16:25 A 32Gb/s, 4.7p.J/bit Optical Link with 11.7dBm Sensitivity in 14nm FinFET CMOS A 60 Gb/s 1.9 Pi/bit NRZ Optical-Receiver with Low Latency Digital CDR in 14nm CMOS FINEET 16:50-17:15 A 20 50 W/CMc 80.0 C/c DMM Link	C26-1 National Taiwan Univ. C26-2 ARM C26-3	C26: Processors and SoC 16:00-16:25 A 501mW 7.61Gb/s Integrated Message- Passing Detector and Decoder for Polar- Coded Massive MIMO Systems 16:25-16:50 A 12.4pJ/cycle Sub-Threshold, 16pJ/cycle Near- Threshold ARN Cortex-M0+ MCU with Autonomous SRPGDVPS and Temperature Tracking Clocks 16:50-17:15	T15-2 Seoul National Univ. T15-3 Chuo Univ. T15-4 GLOBALFO UNDRIES T17-1 GLOBALFO UNDRIES T17-2 CEA-LETI T17-3	14:25-14:50 First Demonstration of Diode-Type 3-D NAN Slope 14:50-15:15 Flash Reliability Boost Huffman Coding (FR Distribution Modulation to Enhance Data-Re 15:15-15:40 CMOS-Embedded STT-MRAM Arrays in 2x T17: CMOS 1 16:00-16:25 Low-Variation SRAM Bitcells in 22nm FDSC 16:25-16:50 Impact of Strain on Access Resistance in Pl 16:50-17:15	ND Flash Memory String Having Super-Steep Switching RBH): Co-Optimization of Data Compression and V _{TH} etention Time by Over 2900x www.science.com www.science.com www.science.com www.science.com <a a="" href="https://www.science.com" www.science.com"="" www.science.com<=""> <a a="" href="https://www.science.com" www.science.com"="" www.science.com<=""> <a a="" href="https://www.science.com" wwww.science.com<=""> <a a="" href="https://www.science.com" www.science.com<=""> <a a="" href="https://www.science.com" www.science.com<=""> <a a="" href="https://wwww.science.com" www.science.com<=""> <a href="https://wwwwwwwwwwwwwwwwwwwwwwwwwwwwwwwwwww</td><td>IBM
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Univ. of
Singapore</td><td>VLSI Integrated Circuit Variability 14:25-14:50 Sub-10<sup>3</sup> 0.cm<sup>2</sup> Contact Resistivity on p-SiGe Achieved by Ga Doping and Nanosecond Laser Activation 14:50-15:15 Highly-Selective Superconformal CVD Ti Silicid Process Enabling Area-Enhanced Contacts for Next-Generation CMOS Architectures 15:15-15:40 Record Low Specific Contact Resistivity (1.2×10<sup>9</sup> 0-cm<sup>3</sup>) for P-7ype Semiconductors: Incorporation of Sr into Ge and <i>In-Situ</i> Ga Doping</td></tr><tr><td>C24-4 17:15-17:40 C25-4 17:15-17:40 T2:15-17:40 T2:15-17:40 Univ. of
Michigan A:7.1JW Switched-Bias MEMS Microphone
Praemplifier for Ultra-Low-Power Voice A:26-Gb/s.8.1-mW Receiver with Linear
Sampling Phase Detector for Data and
Edge Equalization Tsinghua
for Normability-OF Operations with 3.9 Faster Running
Univ. C26-4 17:15-17:40 Influence of Stress Induced CT Local Layout Effect (LLE) on 14nm FinFET Univ. of
Nichigan C25-5 17:40-18:05 C26-5 17:40-18:05 T2:15-17:40 Distribution C25-7 17:40-18:05 C26-5 17:40-18:05 T2:15-17:40 Distribution A:80-5Gb/s Transceiver Using Quarter-Rate
C100-BLFG Univ. of
Platform Power Manager and SIP T2:15-17:40 BM Stacked Nanosheet Gate-All-Around Transistor to Enable Scaling Beyond FinFET</td><td>14:00-15:40</td><td>DENSO
C22-3
Univ. of
Edinburgh
C22-4
Univ. of
Michigan
C24-1
C24-2
CEA-LETI
C24-3
Univ. of</td><td>14:25-14:50 (Invited)
An Imager Using 2-D Single-Photon
Avalanche Diode Array in 0.18-µm CMOS
for Automotive LIDAR Application
14:50-15:15
A 16.5 Giga Events/s 1024 × 8 SPAD Line
Sensor with Per-Pixel Zoomable 50ps-
6.4ns/bin Histogramming TDC
15:15-15:40
A 272.49 µ/jxel CMOS Image Sensor with Embedded
Object Detection and Bio-Inspired 2D Optic Flow Generation
for Nano-Air-Veidie Navigation
C24: Physical Sensors
16:00-16:25
A 10.1<sup>+</sup> 56-Channel, 183 uWelectrode, 0.73 mm<sup>7</sup>sensor
High SNR 3D Hover Sensor Based on Enhanced Signal
Refining and Fine Error Calibrating Techniques
16:25-16:50
A Robust and Versatile, -40°C to +180°C, 8Sps
to 1KSps, Multi Power Source Wireless Sensor
System for Aeronautic Applications
16:50-17:15
A 6K5×41mm<sup>3</sup> General Purpose Audio</td><td>C23-2
C23-2
C23-3
Univ. of
California,
Berkeley
C23-4
Renesas
Electronics
C25-1
IBM T.J.
Research
C25-2
IBM
Research
C25-3
NTT</td><td>14:25-14:50
A 230-260GHz Wideband Amplifier in 65nm
CMOS Based on Dual-Peak G<sub>max</sub>-Core
14:50-15:15
A 65nm CMOS I/Q RF Power DAC with 24
- 42dB 3'<sup>d</sup> Harmonic Cancellation and up to
18dB Mixed-Signal Filtering
15:15-15:40
A 43%-Efficiency 20dBm Sub-GHz Transmitter
Employing Rise-Edge-Synchronized Harmonic
<sup>1</sup>-
Calibration with 33.3% Duty Cycle
5: High-Speed Wireline Circuits
16:00-16:25
A 32Gb/s, 4.7pJ/bit Optical Link with –
11.7dBm Sensitivity in 14nm FinFET
CMOS
16:25-16:50
A 60 Gb/s 1.9 Pj/bit NRZ Optical-Receiver
with Low Latency Digital CDR in 14nm
CMOS FinFET
16:50-17:15
A 2.25-mW/Cb/s 80-Gb/s-PAM4 Linear
Driver with a Single Supply Using Starked</td><td>C26-1
National
Taiwan
Univ.
C26-2
ARM
C26-3
Univ. of
California</td><td>C26: Processors and SoC
16:00-16:25
A 501mW 7.61Gb/s Integrated Message-
Passing Detector and Decoder for Polar-
Coded Massive MIMO Systems
16:25-16:50
A 12:4pJ/cycle Sub-Threshold, 16pJ/cycle Near-
Threshold ARN Cortex-M0+ MCU with Autonomous
SRPGD/VFS and Temperature Tracking Clocks
16:50-17:15
A 2.267 Gbps, 93.7pJ/b Non-Binary LDPC</td><td>T15-2 Seoul National Univ. T15-3 Chuo Univ. T15-4 GLOBALFO UNDRIES T17-1 GLOBALFO UNDRIES T17-2 CEA-LETI T17-3 CEA-I FTI</td><td>14:25-14:50
First Demonstration of Diode-Type 3-D NAN
Slope
14:50-15:15
Flash Reliability Boost Huffman Coding (FR
Distribution Modulation to Enhance Data-Rel
15:15-15:40
CMOS-Embedded STT-MRAM Arrays in 2x
T17: CMOS I
16:00-16:25
Low-Variation SRAM Bitcells in 22nm FDSC
16:25-16:50
Impact of Strain on Access Resistance in Pl
16:50-17:15
Key Process Steps for High Performance at</td><td>ND Flash Memory String Having Super-Steep Switching RBH): Co-Optimization of Data Compression and V<sub>TH</sub> etention Time by Over 2900x c nm Nodes for GP-MCU Applications Integration II DI Technology lanar and Nanowire CMOS Devices nd Reliable 3D Sequential Integration</td><td>IBM
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imec
T16-3
IBM
Research
T16-4
National
Univ. of
Singapore</td><td>VLSI Integrated Circuit Variability 14:25-14:50 Sub-10<sup>3</sup> 0.cm<sup>2</sup> Contact Resistivity on p-SiGe Achieved by Ga Doping and Nanosecond Laser Activation 14:50-15:15 Highly-Selective Superconformal CVD Ti Silicid Process Enabling Area-Enhanced Contacts for Next-Generation CMOS Architectures 15:15-15:40 Record Low Specific Contact Resistivity (1.2×10<sup>4</sup> Ω-cm<sup>2</sup>) for P-Type Semiconductors: Incorporation of Sr into Ge and <i>In-Situ</i> Ga Doping</td></tr><tr><td>Univ. of Michigan Preamplifier for Ultra-Low-Power Voice Xilinx Sampling Phase Detector for Data and Education Univ. Sampling Phase Detector for Data and Education Univ. Sampling Phase Detector for Data and Education Univ. Shortaine 2004 State Running Speed and 11 Higher Energy Efficiency Using Paser Running Pase</td><td>14:00-15:40</td><td>DENSO
C22-3
Univ. of
Edinburgh
C22-4
Univ. of
Michigan
C24-1
KAIST
C24-2
CEA-LETI
C24-3
Univ. of
Michigan</td><td>14:25-14:50 (Invited) An Imager Using 2-D Single-Photon Avalanche Diode Array in 0.18-µm CMOS for Automotive LIDAR Application 14:50-15:15 A 16.5 Giga Events/s 1024 × 8 SPAD Line Sensor with Per-Pixel Zoomable 50ps- 6.4ns/bin Histogramming TDC 15:15-15:40 A 272.49 µb/kel CMOS Image Sensor with Embedded Object Detection and Bio-Inspired 2D Optic Flow Generation ror Nano-Air-Veidle Navigation C24: Physical Sensors 16:00-16:25 A 10.1 56-Channel, 183 UWelectode, 0.73 mm<sup>7</sup>sensor High SNR 3D Hover Sensor Based on Enhanced Signal Refining and Fline Error Calibrating Techniques 16:25-16:50 A Robust and Versatile, -40°C to +180°C, 8Sps to 1KSps, Multi Power Source Wireless Sensor System for Aeronautic Applications 16:50-17:15 A 6x5x4mm<sup>3</sup> General Purpose Audio Sensor Node with a 4.7µW Audio Processina IC</td><td>C23-2
KAIST
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Univ. of
California,
Berkeley
C23-4
Renesas
Electronics
C25-4
IBM T. J.
Watson
Research
C25-2
IBM
Research
C25-3
NTT</td><td>14:25-14:50
A 230-260GHz Wideband Amplifier in 65nm
CMOS Based on Dual-Peak G<sub>max</sub>-Core
14:50-15:15
A 65nm CMOS I/Q RF Power DAC with 24
- 42dB 3'<sup>rd</sup> Harmonic Cancellation and up to
18:dB Mixed-Signal Filtering
15:15-15:40
A 43%-Efficiency 20dBm Sub-GHZ Transmitter
Employing Rise-Edge-Synchronized Harmonic
<sup>1</sup>Calibration with 33.3% Duty Cycle
5: High-Speed Wireline Circuits
16:00-16:25
A 32Gb/s, 4.7pJ/bit Optical Link with –
11.7dBm Sensitivity in 14nm FinFET
CMOS
16:25-16:50
A 60 Gb/s 1.9 Pj/bit NRZ Optical-Receiver
with Low Latency Digital CDR in 14nm
CMOS FinFET
16:50-17:15
A 2.25-mW/Gb/s 80-Gb/s-PAM4 Linear
Driver with a Single Supply Using Stacked
Current-Mode Architecture in 65-nm CMOS</td><td>C26-1
National
Taiwan
Univ.
C26-2
ARM
C26-3
Univ. of
California,
Los Angeles</td><td>C26: Processors and SoC
16:00-16:25
A 501mW 7.61Gb/s Integrated Message-
Passing Detector and Decoder for Polar-
Coded Massive MIMO Systems
16:25-16:50
A 12:4pJ/cycle Sub-Threshold, 16pJ/cycle Near-
Threshold ARM Cortex-M0+ MCU with Autonomous
SRPG/DVFS and Temperature Tracking Clocks
16:50-17:15
A 2:267 Gbps, 93.7pJ/b Non-Binary LDPC
Decoder for Storage Applications</td><td>T15-2 Seoul National Univ. T15-3 Chuo Univ. T15-4 GLOBALFO UNDRIES T17-1 GLOBALFO UNDRIES T17-2 CEA-LETI T17-3 CEA-LETI</td><td>14:25-14:50
First Demonstration of Diode-Type 3-D NAN
Slope
14:50-15:15
Flash Reliability Boost Huffman Coding (FR
Distribution Modulation to Enhance Data-Ref
15:15-15:40
CMOS-Embedded STT-MRAM Arrays in 2x
T17: CMOS I
16:00-16:25
Low-Variation SRAM Bitcells in 22nm FDSC
16:25-16:50
Impact of Strain on Access Resistance in Pl
16:50-17:15
Key Process Steps for High Performance an</td><td>ND Flash Memory String Having Super-Steep Switching RBH): Co-Optimization of Data Compression and V<sub>TH</sub> etention Time by Over 2900x c nm Nodes for GP-MCU Applications Integration II OI Technology Ianar and Nanowire CMOS Devices Ind Reliable 3D Sequential Integration</td><td>IBM
Research
T16-2
imec
T16-3
IBM
Research
T16-4
National
Univ. of
Singapore</td><td>VLSI Integrated Circuit Variability 14:25-14:50 Sub-10<sup>3</sup> 0.cm<sup>2</sup> Contact Resistivity on p-SiGe Achieved by Ga Doping and Nanosecond Laser Activation 14:50-15:15 Highly-Selective Superconformal CVD Ti Silicid Process Enabling Area-Enhanced Contacts for Next-Generation CMOS Architectures 15:15-15.40 Record Low Specific Contact Resistivity (1.2×10<sup>6</sup> Q-cm<sup>3</sup>) for P-Type Semiconductors: Incorporation of Sr into Ge and <i>In-Situ</i> Ga Doping</td></tr><tr><td>Michigan Edge Equilization Univ. Speed and 11 Higher Energy Encome/Using 14 Higher</td><td>14:00-15:40</td><td>DENSO
C22-3
Univ. of
Edinburgh
C22-4
Univ. of
Michigan
C24-1
C24-2
CEA-LETI
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Michigan
C24-4</td><td>14:25-14:50 (Invited)
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Sensor with Per-Pixel Zoomable 50ps-
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15:15-15:40
A 272.40 pJ/kel CMOS Image Sensor with Embedded
Object Detection and Bio-Inspired 2D Optic Flow Generation
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C24: Physical Sensors
16:00-16:25
A 10.1 56-Channel, 183 UWelectode, 0.73 mm<sup>7</sup>sensor
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Berkeley
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https://www.america.com https://www.america.com Integration II DI Technology Hanar and Nanowire CMOS Devices Ind Reliable 3D Sequential Integration	IBM Research T16-2 imec T16-3 IBM Research T16-4 National Univ. of Singapore	VLSI Integrated Circuit Variability 14:25-14:50 Sub-10 ³ 0.cm ² Contact Resistivity on p-SiGe Achieved by Ga Doping and Nanosecond Laser Activation 14:50-15:15 Highly-Selective Superconformal CVD Ti Silicic Process Enabling Area-Enhanced Contacts for Next-Generation CMOS Architectures 15:15-15:40 Record Low Specific Contact Resistivity (1.2×10 ⁶ q.cm ³) for P-Type Semiconductors: Incorporation of Sr into Ge and <i>In-Situ</i> Ga Doping
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