A 120mW Embedded 3D Graphics Rendering Engine with 6Mb Logically Local Frame-Buffer and 3.2GByte/s Run-time Reconfigurable Bus for PDA-Chip

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An embedded 3D graphics rendering engine is implemented as a part of a mobile PDA-chip. 6Mb embedded DRAM macros attached to 8-pixel-parallel rendering logic are logically localized with 3.2GByte/s run-time reconfigurable bus, by which the area is reduced by 25%. Polygon-dependent access to eDRAM macros with line-block mapping reduces the power consumption by 70% with the read-modify-write data transaction. The engine with 2.22Mpolygons/s drawing speed was fabricated using 0.18μm CMOS embedded memory logic technology. Its area and power consumption are 24mm^2 and 120mW, respectively.