C10p2.
Low Power Motion Compensation Block IP with embedded DRAM Macro for Portable Multimedia Applications

Chi-Weon Yoon, Jeonghoon Kook, Ramchan Woo, Se-Joong Lee, Kangmin Lee,
and Hoi-Jun Yoo
Semiconductor System Lab. Dept. of Electrical Engineering, KAIST, Taejon, Korea

Abstract

A 16.3mW motion compensation (MC) block IP with 1.125Mbit embedded DRAM macro is implemented for portable video applications. Its frequency is lowered to 20MHz for low power consumption. In addition, external data I/O is eliminated by integrating DRAM for frame buffers. Distributed nine-tiled mapping (DNTM) with partial activation control (PAC) scheme reduces power for accessing frame buffer up to 31% compared with a conventional 1-bank tiled mapping. Adaptive fetch control (AFC) scheme reduces power up to 29% by eliminating unnecessary switching in the datapath.