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A Floating-Body Charge Monitor Circuit for Partially Depleted SOI CMOS

J.B. Kuang[1], M.J. Saccamango[2], and S. Ratanaphanyarat[3]

IBM Corporation, Advanced Server Development
[1]Rochester, MN 55901, U.S.A.
[2]Poughkeepsie, NY 12601, U.S.A.
[3]formerly with IBM, presently with TSMC North America, San Jose, CA 95134, U.S.A.

Abstract

This paper presents a floating-body charge monitor technique, which does not require the use of body contacts. This technique improves the performance and timing robustness of MUX-type and SRAM bit line circuits on partially depleted (PD) SOI CMOS by minimizing the delay variation due to parasitic bipolar current. It can also be used as a calibration tool for SOI device models by virtue of its direct body charge monitoring and iterative body potential comparison scheme.