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480ps 64-bit Race Logic Adder

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In this paper, a high-speed 64-bit carry look-ahead adder is implemented by Race Logic for fast carry generation. G^1g/G^1k (Level 1 Group Generate/Kill) and G^2g/G^2k (Level 2 Group Generate/Kill) stages are designed by Race Logic. The adder consists of 4-stages, and clk-S63 delay is 480ps with 0.18μm CMOS technology.