DRAM scaling-down to 0.1 μm generation using bitline spacerless storage node SAC and RIR capacitor with TiN contact plug

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A novel bitline spacerless storage node self-aligned-contact (SAC) is developed with the integration of TiN contact plug and Ru/Ta_2O_5/Ru (RIR) capacitor for high density stand-along and embedded DRAMs. For the giga-bit DRAM with design rule of 0.1 μm, spacerless storage node SAC, TiN contact plug and RIR capacitor take a important role in overcoming integration limits with good electrical properties.