Abstract

In traditional design flows the temperature of the chip is assumed to be uniform across the substrate. This paper introduces the modeling and analysis of non-uniform substrate temperature and its effect on the signal integrity. Using a novel non-uniform temperature-dependent analytical distributed RC interconnect delay model, the thermally dependent signal integrity metrics, i.e. signal delay and clock skew, are analyzed. Some design techniques are also provided to eliminate the non-uniform temperature-dependent clock skew in high performance designs.