# A High Performance 100 nm Generation SOC Technology [CMOS IV] for High Density Embedded Memory and Mixed Signal LSIs

K. Miyashita, T. Nakayama, A. Oishi, R. Hasumi, M. Owada, S. Aota, Y. Okayama*, M. Matsumoto, H. Igarashi, T. Yoshida, K. Kasai*, T. Yoshitomi, Y. Fukaura*, H. Kawasaki*, K. Ishimaru*, K. Adachi, M. Fujiwara, K. Ohuchi, M. Takayanagi, H. Oyamatsu, F. Matsuoka, T. Noguchi and M. Kakumu

System LSI Division, *Memory Division, Semiconductor Company, Toshiba Corporation

8 Shinsugita-cho, Isogo-ku, Yokohama, 235-8522, Japan

**Abstract**

This paper demonstrates a 100 nm generation SOC technology [CMOS IV] for the first time. Three types of core devices are presented with optimized gate oxynitrides for their stand-by power conditions. This advanced LOGIC process is compatible with 0.18 $\mu m^2$ trench capacitor DRAM and 1.25 $\mu m^2$ 6 Tr. SRAM. Two kinds of high $V_{dd}$ devices can be prepared by triple gate oxide process. Moreover, for mixed signal applications, $Ta_2O_5$ MIM capacitors are introduced into Cu and low-k interconnects.