Asymmetric Source/Drain Extension Transistor Structure for High Performance Sub-50nm Gate length CMOS Devices

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We present for the first time asymmetric source/drain extension (SDE) transistor structure which can achieve high I_{DSAT} at gate dimensions below 50nm. We demonstrate that this structure alleviates the severe I_{DSAT} degradation reported in literature for devices when gate to source/drain overlap dimensions are reduced to below ~20nm/side. SDE regions are formed by ion implantation and a subsequent drive-in anneal. Fundamental principles of device operation of asymmetric SDE transistor are presented followed by an in-depth analysis of electrical characteristics and associated trade-offs.