A Strategy for Long Data Retention Time of 512Mb DRAM with 0.12μm Design Rule

Hyung Soo Uh, J.K.Lee, S.H.Lee, Y.S.Ahn, H.O.Lee, S.H.Hong, J.W.Lee, G.H.Koh, G.T.Jeong, T.Y.Chung, and Kinam Kim

Technology Development Team, Semiconductor R&D Center, Samsung Electronics Co.
San #24, Nongseo-Ri, Kiheung-Eup, Yongin-City, Kyunggi-Do, 449-900, Korea

Data retention time has been investigated for the mass-productive 512M DRAM with 0.12μm design rule. Cell junction leakage components were for the first time analyzed by using test structure. It was found that process-induced trap density and electric field at the storage node(SN) junction should be reduced to control leakage current and thus data retention time. Moreover, we propose a novel cell transistor using *LOcalized Channel and Field Implantation(LOCFI)* which greatly suppresses the ion implantation damage and reduces the electric field at the same time. Finally, data retention time has been improved by 3~4 times due to the LOCFI cell transistor with optimized process conditions,