Strained Si NMOSFETs for High Performance CMOS Technology

K. Rim, S. Koester, M. Hargrove*, J. Chu, P. M. Mooney, J. Ott,
T. Kanarsky*, P. Ronsheim*, M. Ieong*, A. Grill, H.-S. P. Wong

IBM T. J. Watson Research Center, Yorktown Heights, NY
*IBM Microelectronics Division, Hopewell Junction, NY
phone: 914-945-2946 e-mail: *rim@us.ibm.com*

Performance enhancements in strained Si NMOSFETs were demonstrated at L_{eff} <70 nm. A 70% increase in electron mobility was observed at vertical fields as high as 1.5 MV/cm for the first time, suggesting a new mobility enhancement mechanism in addition to reduced phonon scattering. Current drive increase by ≥35% was observed at L_{eff} <70 nm. These results indicate that strain can be used to improve CMOS device performance at sub-100 nm technology nodes.