50nm SOI CMOS Transistor with Ultra Shallow Junction using Laser Annealing and Pre-Amorphization Implantation

Cheolmin Park, Seong-Dong Kim, *Yun Wang, *Somit Talwar, and Jason C. S. Woo

Department of Electrical Engineering, University of California, Los Angeles, CA 90024, USA
Phone: 1-310-206-3279 Fax: 1-310-206-8495 E-mail: cmpark@ee.ucla.edu
*Verdant Technologies, 3050 Zanker Rd. San Jose, CA 95134

Abstract

CMOS transistors with 50nm physical gate length are fabricated by laser annealing (LA) combining with pre-amorphization implantation (PAI) on SOI substrate. Very low energy laser annealing is required for the SOI substrate, resulting in a large process window margin without undesirable parasitic phenomena. The transistors fabricated by the proposed method show higher drive current and better short channel effect than conventionally rapid thermal annealed (RTA) devices.