High-Density and High-Performance 6T-SRAM for System-on-Chip in 130 nm CMOS Technology

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We have developed the smallest high-density 6T-SRAM cell (1.87 μm^2) reported to date in 130 nm CMOS logic process for System-on-Chip (SOC). We have also developed an ultra-high speed 6T-SRAM cell (2.49 μm^2) with cell current of 116 μA for SOC applications requiring even higher performance. These were achieved using our systematic SRAM technology development methodology and optimized OPC capability. These cells do not require additional process steps and use 248 nm lithography, making them very attractive for low-cost manufacturing of SOCs.