A 4GHz 130nm Address Generation Unit with 32-bit Sparse-tree Adder Core

Sanu Mathew, Mark Anders, Ram K. Krishnamurthy and Shekhar Borkar

Circuits Research, Intel Labs, Intel Corporation, Hillsboro, OR 97124, USA, sanu.k.mathew@intel.com

This paper describes a 32-bit Address Generation Unit (AGU) designed for 4GHz operation in 1.2V, 130nm technology. The AGU utilizes a 152ps dual-V_t sparse-tree adder core to achieve 20% delay reduction, 80% lower interconnect density and a low (1%) active energy leakage component. The semi-dynamic implementation enables an average energy profile similar to static CMOS, with good sub-130nm scaling trend.