

0.4-V Logic Library Friendly SRAM Array Using Rectangular-Diffusion Cell and Delta-Boosted-Array-Voltage Scheme

Masanao Yamaoka, Kenichi Osada, and Koichiro Ishibashi*

Central Research Laboratory, Hitachi, Ltd., Kokubunji, Tokyo, 185-8601, Japan

*Presently with Semiconductor Technology Academic Research Center (STARC)

Phone: +81-42-323-1111, Fax: +81-42-327-7680, E-mail: yamaokam@crl.hitachi.co.jp

We designed a logic library friendly SRAM array. The array uses rectangular-diffusion cell (RD-cell) and delta-boosted-array-voltage scheme (DBA-scheme). In the RD-cell, the cell ratio is 1.0, and it reduces the imbalance of the cell ratio. A low supply voltage deteriorates the static noise margin, however, the DBA-scheme compensates it. Using the combination of RD-cell and DBA-scheme, a 32-kB test chip achieves 0.4-V operation at 4.5-MHz frequency and 140- μ W power dissipation and 0.9- μ A standby current.