

Design Optimizations of a High Performance Microprocessor Using Combinations of Dual- V_T Allocation and Transistor Sizing

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Joint optimizations of dual- V_T allocation and transistor sizing for a high performance microprocessor reduce low- V_T usage by 36%-64%, compared to a design where only dual- V_T allocation is optimized. Designs optimized for minimum power (DVT+S) and minimum area (L-SDVT) reduce leakage power by 20%, with minimal impact on total power and die area. An enhancement of the optimum DVT+S design allows processor frequency to be increased efficiently during manufacturing through low- V_T device leakage push only.