

Power Dissipation Issues in Interconnect Performance Optimization for Sub-180 nm Designs

This paper presents a novel methodology to calculate the buffer size and the inter-buffer separation, which minimizes the total interconnect power dissipation for any given performance penalty criteria. The methodology is applied to calculate the power-optimal buffering schemes for various ITRS technology nodes for a 5% delay penalty. Furthermore, it is shown that short-circuit and leakage power are important components of the total power dissipation and ignoring them in power optimization can lead to large errors for sub-180 nm designs.