A Transition-Encoded Dynamic Bus Technique for High-Performance Interconnects

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A transition-encoded dynamic bus technique enables interconnect delay reduction while maintaining the robustness and switching energy behavior of a static bus. Efficient circuits, designed for a drop-in replacement, enable significant delay and peak-current reduction even for short buses, while obtaining energy savings at aggressive delay targets. In a 180nm 32-bit microprocessor, 79% of all global buses exhibit 10%-35% performance improvement.