A Monolithic CMOS 10.4-GHz Phase Locked Loop

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A 10.4-GHz PLL with a 256/257 dual modulus prescaler implemented in a 0.18-μm CMOS process is presented. The prescaler with a 4/5 synchronous counter operates up to 14 GHz. The counter achieves this by using feedback. The phase noise levels of the PLL and VCO at a 3-MHz offset with I_{vco}=8.1mA are -122 dBc/Hz. The PLL operates between 9.7 and 10.4 GHz, while consuming 34mA at V_{DD}=1.8V.