1.2Gbps/pin Simultaneous Bidirectional Transceiver Logic with Bit Deskew Technique

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A simultaneous bidirectional transceiver logic - composed of a transmitter with an output level feedback pre-buffer and a receiver with two sense amplifiers and a hazard-free selector - reduced the data jitter originating from three voltage level transmission. A bit deskew technique that takes into account the influence of switching noise also enabled to obtain the maximum timing margin. Stable throughput of 1.2Gbps/pin was achieved in simultaneous 81-pin operation using a printed circuit board.