Four-Way Processor 800 MT/s Front Side Bus with Ground Referenced Voltage Source I/O

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A 40cm multi-drop bus shared by 5 test chips to emulate 4 processors and a chipset runs error free at 800MT/s with 130mV margin using Ground Referenced Voltage Source (GRVS) I/O scheme. For comparison, when the same test chip is programmed to use Gunning Transceiver Logic (GTL), the bus speed is 500 MT/s for the same 130mV margin under identical conditions.