A low-power, high-speed and high-density 100 nm CMOS technology is developed for very-low-voltage operation, by using 193nm lithography, high-performance transistors with sidewall notch, high-density 6-T SRAM cell ($1.16um^2$) and Cu/VLK interconnect ($k_{eff}$=3). High-performance transistors with sidewall notch to reduce overlap and junction capacitance and Cu/VLK interconnect with low-k SiC barrier realize higher circuit speed by 10% and lower power consumption by 80%, compared to 130nm CMOS technology.