Title of Abstract:

High performance 60nm CMOS technology enhanced with BST (body-slightly-tied) structure SOI and Cu/Low-k (k=2.9) interconnect for microprocessors

Auther :
T. Kudo , S. Miyake, T. Syo, S. Maruyama, Y. Yama, T. Katou,
T. Tanaka*, T. Matuda, M. Ikeda, K. Imai and H. Ooka
ULSI Device Development Divisions, *Microcomputer Divisions, NEC Corporation
1120 Shimokuzawa, Sagamihara, Kanagawa 229-1198, Japan
Tel: +81-42-771-0861, Fax: +81-42-771-0938, E-mail: t-kudo@ak.jp.nec.com

Abstract:
We have developed high performance / low active power CMOS technology for microprocessor products. This features 1) drive current enhancement with high-dose low-energy I/I for S/D extension, 2) body-slightly-tied (BST) CMOS/SOI with partial trench isolation and local channel doping, 3) Cu interconnect with low-k (k=2.9) dielectric. BST CMOS/SOI shows negligible history effect, therefore existing circuit and layout design of bulk CMOS are reusable while enjoying all advantages of SOI.