70 nm Fully-Depleted SOI CMOS Using a New Fabrication Scheme: The Spacer/Replacer Scheme

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High-performance Fully-Depleted SOI CMOS transistors have been realized on a 28 nm ultra thin silicon substrate with a physical gate length of 70 nm and a post NO-annealed gate oxide of 14 Å. A new fabrication scheme, the *Spacer/Replacer* scheme, has been used to optimize the device performance of ultra thin-film SOI transistors. Excellent device performance has been obtained: I_{on} equals 711 μA/μm and 350 μA/μm at I_{off} = 16 nA/μm for nMOS and pMOS, respectively. The unloaded ringoscillator gate-delay is 14.5 ps at V_{DD} = 1.2 V.