

Novel DRAM Cell Transistor with Asymmetric Source and Drain Junction Profiles Improving Data Retention Characteristics

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The new cell transistor structure with asymmetric source and drain junction profiles was proposed and fabricated with 0.12 μ m DRAM technology. The junction profile at the storage node was designed to reduce electric field to minimize junction leakage current. On the other hand, the junction profile at the bit-line direct contact node was designed to suppress short channel effects. It is considered to be highly scalable for device scaling and to solve fine printing requirements.