Integration of Capacitor for Sub-100-nm DRAM Trench Technology

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Abstract

Key enabler in scaling DRAM trench capacitors to sub-100nm ground rules is a viable collar integration concept. For the first time, the successful implementation of a buried collar concept is demonstrated, which leaves ample space for the connection from the array device to the inner electrode. The new collar scheme is compatible with capacitance enhancement techniques, e.g. HSG and high-k node dielectrics. In addition, a metal fill of the trench, necessary to maintain a low series resistance of the trench fill, is demonstrated for the first time. The successful integration in trenches is presented.