A Highly Manufacturable 110nm DRAM Technology with $8F^2$ Vertical Transistor Cell for 1Gb and Beyond

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This paper describes a 110nm half-pitch DRAM technology utilizing an $8F^2$ vertical transistor trench cell and optimized for ease of manufacturing. All four critical lithography steps are regular patterns in the array. High performance is provided through the use of tungsten Word-Lines, tungsten Bit-Lines, and the double-gated vertical array transistors. Area enhancement techniques in the trench capacitor allow the use of conventional dielectric materials into the 110nm generation. A 512Mb prototype chip has been fabricated using this technology.