

Strong Correlation between Dielectric Reliability and Charge Trapping in SiO₂ / Al₂O₃ Gate Stacks with TiN Electrodes

A. Kerber^{1,4,5}, E. Cartier^{2,4}, R. Degraeve³, L. Pantisano³, Ph. Roussel³, G. Groeseneken³

¹ Infineon Technologies AG, ² IBM Research Division, ³ IMEC,
⁴ International Sematech assignee at IMEC, ⁵ Institut für Halbleitertechnik TU-Darmstadt
c/o IMEC, Kapeldreef 75, B-3001 Leuven, Belgium
phone: +32 (16) 288-183, fax: +32 (16) 281-844, e-mail: Andreas.Kerber@imec.be

Abstract

Polarity-dependent charge trapping and defect generation have been observed in SiO₂ / Al₂O₃ gate stacks with TiN electrodes. For the substrate injection case, electron trapping in the bulk of the Al₂O₃ films dominates, whereas hole trapping near the Si substrate is observed for gate injection. This asymmetry in defect creation causes an asymmetry in oxide reliability. For gate injection, reliability is limited by the thin SiO₂ interfacial layer, yielding low beta values, independent of the Al₂O₃ thickness. For substrate injection, reliability is limited by electron trap generation in the bulk of the Al₂O₃ film, yielding a strong thickness dependence of the beta values, as expected from the percolation model and as observed in SiO₂ layers of similar thickness.