An Adaptive Reference Generation Scheme for 1T1C FeRAMs

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A reference time, instead of a reference voltage, is generated and used to compare stored "0" and "1" in a race of bitlines towards reaching a threshold voltage in a 1T1C FeRAM. The reference time is adaptive, tracking process variations, aging, and fatigue of ferroelectric capacitors. This scheme is implemented in a 256x128-bit testchip in a 0.35 μm ferroelectric process and achieves a 40 ns access time at 3 V.