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10 GHz, 20mW, fast locking, adaptive gain PLLs with on-chip Frequency Calibration for agile frequency synthesis in a 0.18μm digital CMOS process

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Abstract

This paper describes two fully integrated 10GHz PLLs with an LC-VCO implemented in a 0.18μm native digital CMOS process. In the first version, an adaptive gain circuit along with a wide-swing charge pump improves the lock range and ensures faster settling. The PLL has a 1.6GHz tuning range, a 0.5μs settling time (for a frequency step equal to 10% of the tuning range), reference sideband power of –58dBc and phase noise of –105dBc/Hz at a 10kHz offset and –120dBc/Hz at a 20MHz offset (rms jitter of 1.3ps) while dissipating less than 20mW from a 1.6V power supply. Enhancing the process with deep n-wells appears to improve the noise isolation of the circuit by about 5dB. The second variant incorporates a combination of coarse and fine tuning for the VCO along with a new frequency calibration circuit based on a digital quadri-correlator. This PLL has a 1.25GHz tuning range, a 10μs settling time, a reference sideband power below the noise floor and a phase noise of –105dBc/Hz at 10kHz and –130dBc/Hz at 20MHz from the carrier (rms jitter of 1.2ps).