A 90nm 6.5GHz 256x64b Dual Supply Register File with Split Decoder Scheme

Steven Hsu, Bhaskar Chatterjee*, Manoj Sachdev*, Atila Alvandpour, Ram K. Krishnamurthy, Shekhar Borkar

Circuits Research, Intel Labs, Intel Corporation, Hillsboro, OR 97124, USA, ramk@ichips.intel.com

*University of Waterloo, Ontario N2L3G1, Canada, bhaskar@vlsi.uwaterloo.ca

Abstract

This paper describes a 256x64b 2-read, 1-write ported static register file for 6.5GHz operation in 1.2V, 90nm CMOS. Read/write select drivers and decoder use 0.9V lower supply to reduce total energy by 23%. Local/global bitlines use a leakage-tolerant split-decoder scheme with conditional precharge to achieve 65% (90%) higher DC robustness compared to conventional static (dynamic) bitline scheme.